A STUDY OF ONE-PORT NEGATIVE RESISTANCE OSCILLATORS UTILIZING FOUR-LAYER DIODES

By

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UTILIZING FOUR-LAYER DIODES

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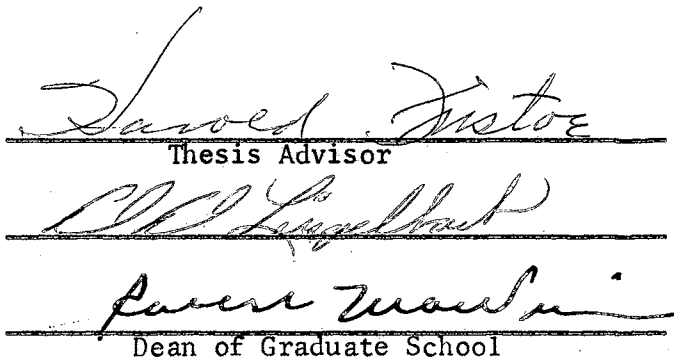

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PREFACE

This thesis reports the work performed by the author in an investigation of the application of graphical techniques to the theory of negative resistance oscillators. The investigation was primarily concerned with determining graphical methods of analyzing and designing oscillator circuits using four-layer semiconductor diodes.

Four-layer diodes have not, at the time of this writing, reached the stage where they can be produced in quantity with any type of consistent characteristics. The wide range of values of the describing parameters associated with four-layer diodes of the same type makes circuit designing quite difficult. The author felt that the application of graphical techniques would be enlightening to the person attempting to use four-layer diodes in oscillators.

While four-layer diodes can easily be made to produce sustained oscillations, it is felt that their main application is in switching circuits, since their characteristics are quite similar to a slightly imperfect switch. Some of the applications of four-layer diodes which have been studied include: monostable, bistable, and astable multivibrators, relaxation oscillators, sine wave oscillators, and pulse generators.

The author would like to express his sincere gratitude to his advisor, Dr. Harold T. Fristoe, for the interest he has shown in this study and for his inspirational advice concerning the writing of this

thesis.

I would also like to express my gratitude to Dr. Fristoe for procurring sample diodes from Texas Instruments, Inc. and to Texas Instruments, Inc. for generously furnishing those samples.

Appreciation is also expressed to John Champ Paul and many other staff members of the Electrical Engineering Department at Oklahoma State University with whom many enlightening discussions were held.

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CHAPTER I

INTRODUCTION

The first extensive treatment of non-linear oscillations was Theory of Oscillations[1], which was published in Russian in 1937 and in English in 1949. This text deals primarily with oscillations in mechanical systems, with some attention being given to electrical systems. With the single exception of the arc discharge, this test is restricted to oscillitory systems employing some type of external feedback to sustain oscillations.

The arc discharge is a classical example of a device which exhibits a region of incremental negative resistance, i.e., a region where a decrease in terminal voltage is associated with an increase in current. Other common devices which exhibit this characteristic are neon tubes, thyratron tubes, unijunction transistors, silicon controlled rectifiers, tunnel diodes, and four-layer diodes. Each of these devices, at some pair of terminals, over some region of their terminal characteristics, is capable of exhibiting an incremental negative resistance.

Two terminal devices which exhibit negative resistance characteristics are divided into two groups.[2] The first of these is called a

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[1]A. A. Andronow and C. E. Chaikin, Theory of Oscillations, Princeton, 1949.

[2]Leonard Strauss, Wave Generation and Shaping, New York, 1960.

current controlled negative resistance device, since its v-i characteristics are single valued with respect to the current. The other type is called a voltage controlled negative resistance device, since its v-i characteristics are single valued with respect to terminal voltage. In general, these two divisions may be taken as being simply duals of one another. Their circuit application can thus be treated in the same manner using the dual of the circuit being considered.

The existence of incremental negative resistance implies that the device may be capable of generating some form of energy without external excitation. In all practical cases, this generated energy is limited by the existence of positive resistance regions which dissipate the energy supplied by the negative resistance.

The four-layer diode is a typical current controlled device which exhibits a region of incremental negative resistance. This device was first conceived by William Shockley at Bell Labs in 1952. The classical model of the four-layer diode has only two terminals, but it was soon discovered that the addition of a third terminal to one of the inner semiconductor layers produced a device with characteristics quite similar to a gas-filled thyratron. One of the distinct advantages of these four-layer devices over their gas tube analouge is that the voltage across the semiconductor device when in the saturation region, is only a few volts, while the corresponding voltage across a gas tube is at least an order of magnitude greater. The extreme non-linearity associated with the v-i characteristics of the four-layer diode and other non-linear resistances prohibits the exclusive application of linear circuit theory. Linear circuit theory may be applied if the v-i characteristics of the device may be accurately approximated by a piecewise linear

curve consisting of linear segments.

Another method of analysis of circuits containing non-linear resistances is to determine an analytical expression, usually in polynomial form, which represents the characteristics over the region of operation. This approach usually involves obtaining the solution of a non-linear differential equation. In general, non-linear differential equations are very difficult to solve.

The purpose of this thesis is to develop graphical techniques for analyzing one-port negative resistance oscillator circuits. This graphical theory will be applied to the actual terminal characteristics of the device and, with the aid of linear circuit theory, allow predictions to be made as to the existence of oscillations and their form. Graphical criteria involving stability and instability of solutions to a given network will be developed as it applies to general current controlled non-linear resistance characteristics. This criteria will then be experimentally verified by analyzing two four-layer diode oscillator circuits.

CHAPTER II

GENERAL THEORY OF ONE-PORT NEGATIVE RESISTANCE OSCILLATORS

The first step in developing a general theory of oscillations utilizing one-port negative resistance devices is to establish necessary conditions for sustained oscillations. The problem of determining sufficient conditions for sustained oscillations can only be approached when these necessary conditions are absolutely satisfied.

Consider the circuit in Figure 1 where one port of an N-port passive network has been connected to a one-port non-linear resistance.

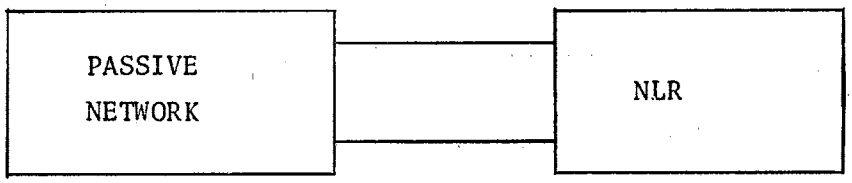

Figure 1. General Non-Linear Resistance Oscillator

Note, that the form of the non-linear resistance is not restricted. Since the passive network will always contain some resistance, it is concluded that the existance of sustained oscillations of any type will require that some form of energy be supplied by the non-linear resistance. Assuming that the non-linear resistance contains no finite energy sources, then it must exhibit a region of incremental negative resistance to the

passive network. Therefore, the existance of positive resistance in the passive network implies that sustained oscillations can exist only if, over some region of the v-i characteristics of the non-linear resistance, the slope of the characteristic is negative.

If the slope of the non-linear resistance's v-i characteristics were negative over its full range of operation, then the non-linear resistance would be capable of supplying an infinite amount of power, hence, the non-linear resistance must include regions of both negative and positive incremental resistance. For brevity, the term non-linear resistance will be abbreviated NLR in the remainder of this investigation. It should also be understood that reference to positive and negative resistance automatically implies incremental resistance.

A second requirement to be imposed upon an oscillatory system is that it be capable of some form of energy storage, hence, the passive network (Figure 1) must contain at least one storage element. This storage element would normally be either an inductance or a capacitor. Lead inductance and stray wiring capacitance may be sufficient in this case.

Two general types of negative resistance characteristics will be considered in this investigation. A voltage controlled non-linear resistance--VNLR--is the name given to a set of v-i characteristics where the current is a single-valued function of voltage. This type of characteristic can be described functionally as $i = i(v)$. The slope of the v-i characteristics is given by

$$\frac{di(v)}{dv} = g(v)$$

where $g(v)$ is a conductance term and is also a function of voltage. In

working with the characteristics, it is better to consider the VNLR as a negative conductance device. The tunnel diode is an example of a two-terminal VNLR device. Typical diode characteristics are shown in Figure 2.

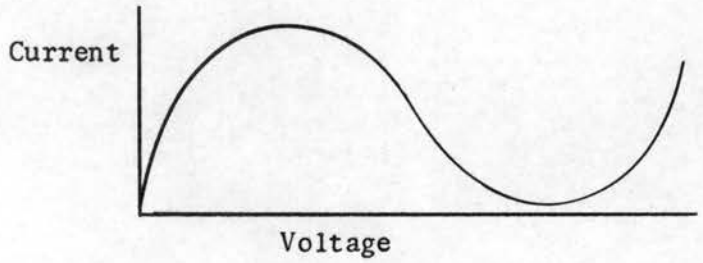

Figure 2. Tunnel Diode V-I Characteristics

A current controlled non-linear resistance--CNLR--is a device in which the voltage across the device is a single-valued function of the current through the device. Functionally, the CNLR characteristics may be represented as $v = v(i)$. The slope of the CNLR characteristics is then given by

$$\frac{dv(i)}{di} = r(i) \ .$$

In each case it is assumed that $i(v)$ and $v(i)$ are each continuously differentiable functions of v and i respectively. Also, the existance of an incremental negative resistance or conductance region is inherently implied by the use of CNLR and VNLR. A unijunction transistor is a device which exhibits CNLR characteristics across its emitter-base terminals under the proper circuit conditions. Typical unijunction transistor input characteristics are shown in Figure 3.

The actual shape of the v-i characteristics of a device may depend upon one or more parameters associated with the device. In the case of a device possessing more than two terminals, the v-i characteristics at

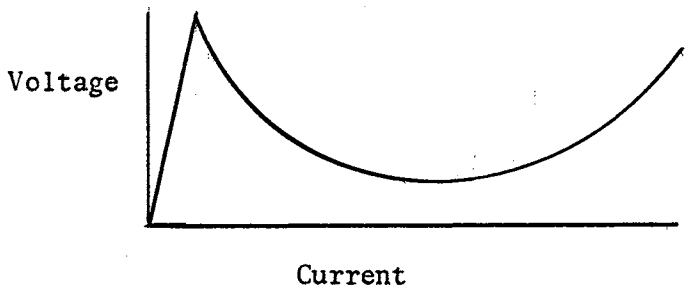

Figure 3. Typical Unijunction Transistor Input V-I Characteristics

one pair of terminals may depend upon the current flow or voltage associated with the other terminals. It is found, for instance, that the v-i characteristics at the emitter-base terminals of a unijunction transistor are actually a family of characteristics dependent upon the collector-base voltage. One-port devices exhibiting CNLR characteristics include the four-layer diode and the familiar neon tube.

In this thesis, ideal constant current and voltage generators will be exclusively employed to supply the initial oscillator excitation and power losses. The passive circuit elements will, of course, be either resistors, inductors, or capacitors. It will soon become apparent that the fundamental mode of operation or oscillation is then completely dependent upon the passive circuitry and the region of operation of the NLR.

As a beginning, consider the circuit in Figure 4. The equation

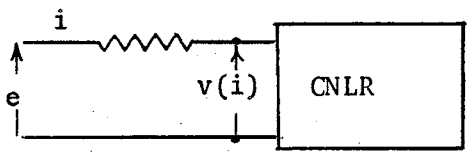

Figure 4. Series Resistance and CNLR Circuit

relating input voltage and current is given by

$$e = iR + v(i)$$

where v(i) is the functional relationship giving the terminal voltage of the CNLR as a function of device current. If the CNLR characteristics are of the form given in Figure 5a, then e = e(i) is found simply by forming the series composite v-i characteristics of Figure 5a and the linear resistance R. Thus, Figure 5b represents the input characteristics of the circuit in Figure 4.

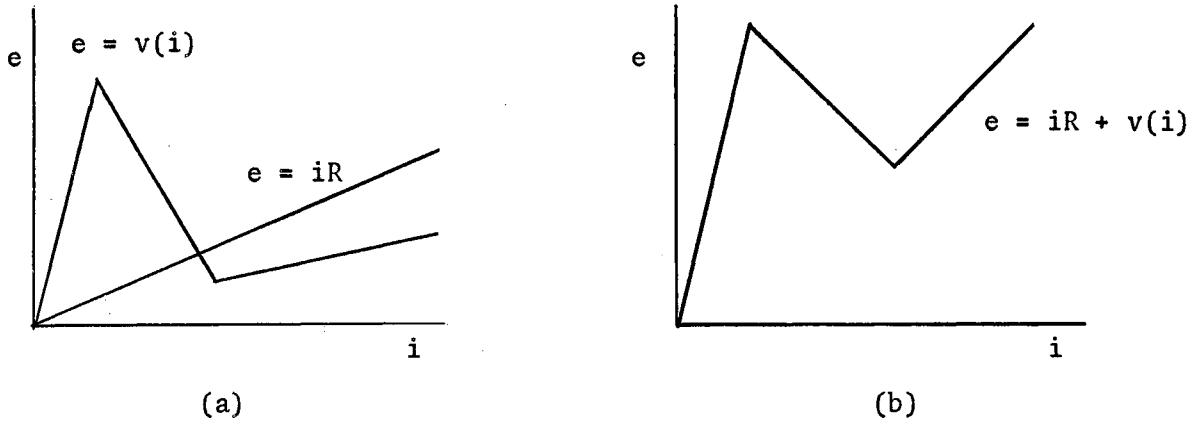

Figure 5. V-I Characteristics of Series Resistance and CNLR

Now, consider the circuit in Figure 6, where E and R are fixed.

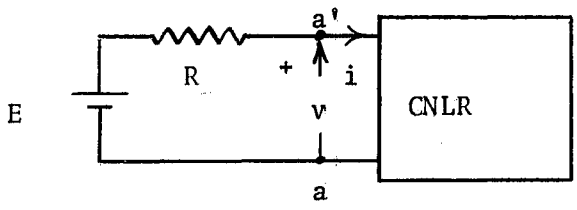

Figure 6. CNLR Bias Circuit

The solution for v(i) is given by

$$v(i) = E - iR \tag{1}$$

which is the familiar load line equation. The load line corresponding to the resistance R and source E is plotted on the CNLR characteristics of Figure 5b in Figure 7.

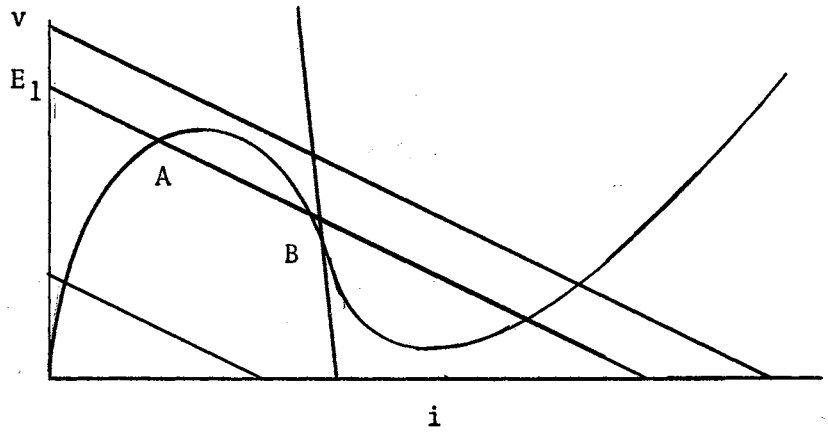

Figure 7. Grpahical Solution of v(i) = E - iR

Equation (1) must at all times be satisfied, therefore as E is varied, the intersection of the two curves will trace out the v - i characteristics of the device. The equation

$$v(i) = E - iR$$

is a two parameter family of straight lines with slope

$$\frac{dv}{di} = - R \quad ,$$

where R is a constant parameter. If R is fixed, then each value of E uniquely determines a straight line which intercepts the voltage axis at v = E and the current axis at i = E/R. When $E = E_1$ (Figure 7),

three possible loci which are solutions to Equation (1) are indicated, since the load line intersects the CNLR characteristics at three points. The analysis and design of NLR oscillators require that an investigation be made concerning the dynamic stability of all possible solutions to Equation (1).

For the purpose of this investigation, dynamic stability will be defined as follows: given a series CNLR circuit with solution point (v_1, i_1). The point (v_1, i_1) is a stable solution if there exists a neighborhood $\underline{N}(i_1; c)$, $c > o$, $i_1 - c > i > i_1 + c$ such that if the current i is perturbed slightly from i_1 by an amount Δi, $|\Delta i| < c$ at some time t_o, then at any time $t > t_o$, i will reamin in $\underline{N}(i_1; c)$. Otherwise, the solution is unstable.

Figure 8 is an enlarged section of Figure 7 showing the solutions of Equation (1) at points A and B. Assume that the circuit is operating at point A, and that at some time t_o a small perturbation of current Δi occurs. This perturbation of current will cause a change in voltage across the resistor R of the amount

$$\Delta v_R = R \ \Delta i$$

and also a change in the voltage across the CNLR device of the amount

$$\Delta v_{CNLR} = \left(\frac{dv(i)}{di}\right)\Bigg|_A \Delta i \ .$$

The total change in voltage across the R and the CNLR device is then

$$\left(R + \frac{dv}{di}\right)\Bigg|_A \Delta i \ .$$

Now, R is always positive, and at point A, $\frac{dv}{di}\Big|_A$ is positive; hence,

the sign of the perturbation of i determines the sign of the total voltage change. Hence, if $\Delta i > 0$, then

$$\left(R + \frac{dv}{di}\right)\Bigg|_A \quad \Delta i > 0 \ .$$

The circuit equation, Equation (1), must at all times be satisfied; hence, a decrease in current must occur to make

$$\left(R + \frac{dv}{di}\right)\Bigg|_A \quad \Delta i$$

approach zero. Point A is thus a point of dynamic stability, in that any slight disturbance of the current in the circuit immediately requires a disturbance in the opposite direction to return the circuit to its original condition.

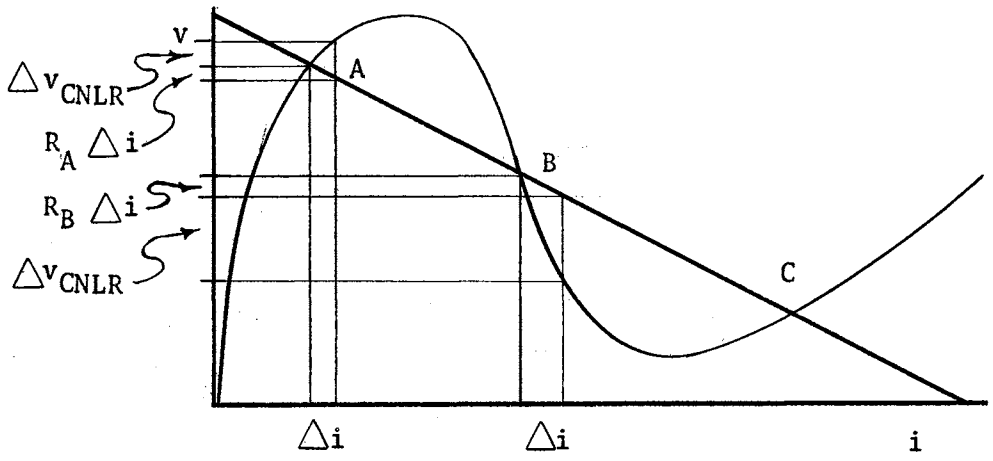

Figure 8. Graphical Determination of the Stability of CNLR Series Circuit

Operation at B is analyzed in exactly the same manner. A perturbation of the current at B results in a total circuit voltage change of

$$\left(R + \frac{dv}{di}\right)\Bigg|_B \quad \Delta i \ .$$

At point B, it is noted that

$$\left.\frac{dv}{di}\right|_B < 0$$

so that if $\Delta i > 0$, then the total voltage change may be either positive or negative, depending upon the relative magnitudes of R and $\left.\frac{dv}{di}\right|_B$. Defining

$$\frac{dv}{di} = -r_d \text{ , } \frac{dv}{di} < 0$$

and taking $\Delta i > 0$, the sign of the total voltage change becomes directly dependent upon the sign of $(R - r_d)$. If $(R - r_d) > 0$, then the point is a point of dynamic stability similar to point A. If $(R - r_d) < 0$, then the total voltage change is negative. To satisfy Equation (1) then, a further increase in current would be required; hence, if $(R - r_d) < 0$, a disturbance in the current would immediately cause an even greater distrubance and therefore operation would rapidly leave the original operating point and quickly come to rest at a stable solution point of the system.

It can be concluded from the above that a series circuit containing a positive linear resistance R and a CNLR is stable only in those regions of the v-i characteristics of the CNLR where the following inequality is satisfied:

$$R + \frac{dv(i)}{di} > 0 \qquad (2)$$

A second conclusion obtained from this stability analysis is that any region of incremental negative resistance must ultimately be bounded by regions of incremental positive resistance, otherwise infinite power

gain would be realized.

If the values of E and R are such that the load line is tangent to the CNLR characteristics, then $R = \frac{dv}{di}$ at the tangent point. A reflection on Figure 8 indicates that the only possibilities for the load line being tangent to the CNLR characteristics occurs in the negative resistance region assuming finite positive R. It is also easily seen that the only possibility of a tangent point being a stable point is for the point to be a point of inflection of the v-i characteristics of the CNLR.

The problem of developing oscillations, while it may seem quite easy, is a formidable problem when required to predict frequency and waveform, eliminate extraneous mode of oscillations, and obtain self-starting oscillations using NLR's. The initial conditions on storage elements, bias point, d-c load, as well as the number and type of storage elements must all be considered in the light of the negative resistance device characteristics in determining the possible modes of oscillations.

Oscillator modes will now be defined in a general sense.

Monostable: A monostable circuit is stable in only one state, an external signal being required to switch to an unstable state. The circuit will return to its one stable state when the external signal is removed.

Bistable: A bistable circuit has two stable states and an external signal is required to cause it to switch states.

Astable: An astable circuit has no stable states and is capable of producing sustained oscillations.

Sinusoidal: A sinusoidal or almost sinusoidal oscillator is an astable circuit, but it must contain at least two different types of storage elements.

Monostable and bistable circuits will not be considered at this time, for they are not capable of sustained oscillations. Typical modes of oscillation which can be produced by astable oscillators are square waves, pulses, and sawtooth sweeps. When the active device is a one-port negative resistance device, each of these modes of oscillation can be obtained with only the addition of a single suitable storage element and bias network.

One possible method of analysis of circuits containing NLR's is through the use of piecewise linear models.[1] This method involves replacing the actual v-i characteristics of a NLR such as shown in Figure 9a with a piecewise linear curve similar to that shown in Figure 9b.

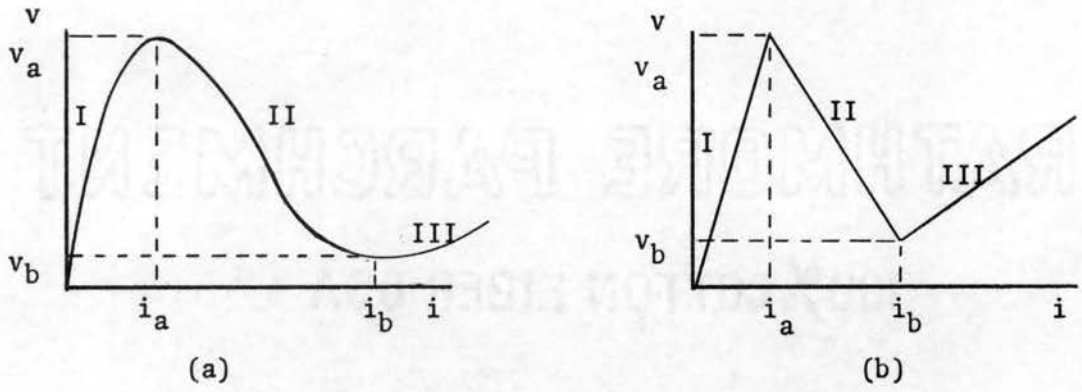

Figure 9. Piecewise Linearization of NLR Characteristics

Analysis of combinations of piecewise linear circuits and single storage

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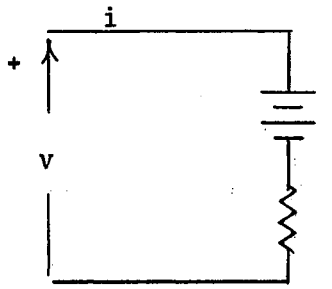
[1] H. J. Zimmermann and S. J. Mason, Electronic Circuit Theory (New York, 1959).

elements can be carried out as in linear circuits.

The incremental resistance of the NLR (Figure 9b) is negative in state II and positive in states I and III. The equivalent circuit of the device when operating in region II is simply a negative resistance of magnitude R_{II} in series with an appropriate voltage source. As an example, the circuit in Figure 10 could represent the device characteristics in Figure 9a for operation over the range of currents $i_a > i > i_b$.



$$E_{II} = \frac{v_b\, i_a - v_a\, i_b}{i_a - i_b}$$

$$r_{II} = \frac{v_a - v_b}{i_a - i_b}$$

Figure 10. Piecewise Linear Model $i_a > i > i_b$

The equation of the characteristics in this region is

$$v = E + iR$$

or

$$v = \frac{(v_b\, i_a - v_a\, i_b)}{(i_a - i_b)} + \frac{(v_a - v_b)}{(i_a - i_b)}\, i$$

which is simply the equation of the straight line of which the region under consideration is a segment. Similar models can be constructed to represent each piecewise linear state. Sequential switches can be employed to switch from one piecewise linear state to another. This type of analysis is very tedious and is only as accurate as the

piecewise linear representation.

Another approach to the problem utilizes a polynomial representation of the v-i characteristics of the NLR. If, for instance, the function v(i) can be represented as

$$v(i) = P(i)$$

then the differential equation, or equations, representing the circuit can be obtained and possibly solved. The inherent problem here is that the degree of the polynomial P(i) is at least three and usually much higher. The resulting differential equations governing the system would be non-linear and very difficult to solve.

A third approach to the problem is a graphical approach utilizing the actual characteristics of the NLR and supplemented with a good working knowledge of the transient behavior of passive circuits and the NLR.

Consider the CNLR characteristic in Figure 11a which has the load line corresponding to the circuit in Figure 11b superimposed upon it. Assuming that R is fixed, then the position of the load line is entirely determined by the bias voltage E. The value of E then determines the operating point of the circuit, subject to the stability criteria established in Equation (2).

This criteria prohibits operation in the negative resistance region between points B and D, for in this region, $R < r_d$. The locus of operation as E is cycled from E_A to E_C and back to E_A is of considerable interest.

Point A is a stable solution to the system, therefore, the path of operation will start at A and follow the CNLR characteristic to point B.

Further increase of E from E_B requires that operation switch immediately to B', since now the load line must intersect the characteristic only at B', which is also a stable point. Operation will then be along the path from B' to C. Decreasing E from E_C will cause operation along the characteristic to B' and on to D, the entire path being in a stable region.

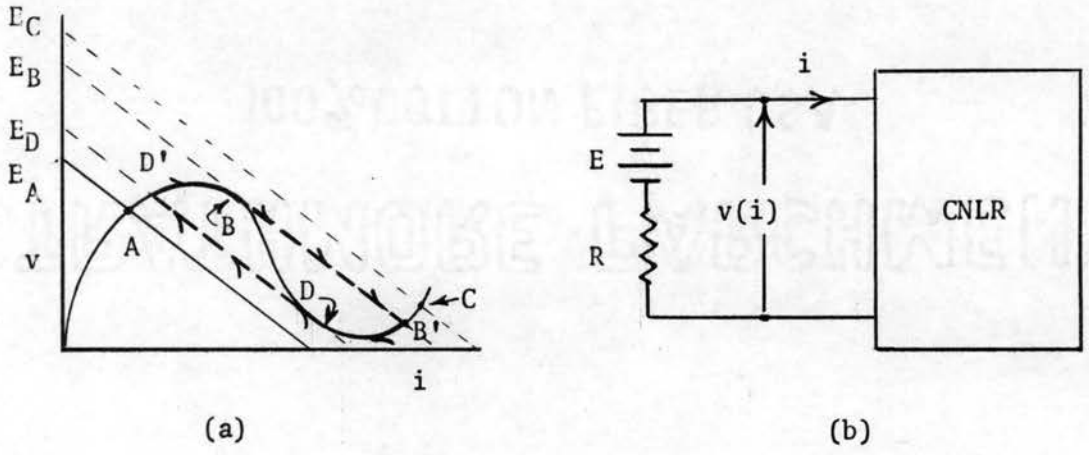


Figure 11. Graphical Solution of CNLR Series Circuit

Further decrease in E from E_D will again require operation to switch from D to D'. If now E is increased just enough for operation to switch to point B' and then decreased until operation just switches to D', the path D'BB'DD' will be the locus of operation. The time required for operation to switch will be limited only by the transient response of the CNLR device, lead inductance and stray capacitance. The effects of these transients will be to curve the switching loci BB' and DD' as well as to impose a finite switching time.

The addition of a storage element to the basic circuit considered in Figure 11 is necessary if sustained oscillations are to be achieved. The type of storage element, whether capacitive or inductive is found

to depend upon the type of NLR used.[2]

Consider the circuit in Figure 12. The terminal voltage across the CNLR is a single valued function of the current through the device. On the other hand, there are as many as three possible values of current which may exist for a given terminal voltage. Thus, the current is a multivalued function of terminal voltage. The current is thus unrestricted in value at a given terminal voltage, and hence an energy storage element must be used which will allow instantaneous changes in current. This prohibits the use of an inductor as a single energy storage element with a CNLR oscillator circuit. The circuit in Figure 13 is therefore taken as the basic oscillator circuit using a CNLR.

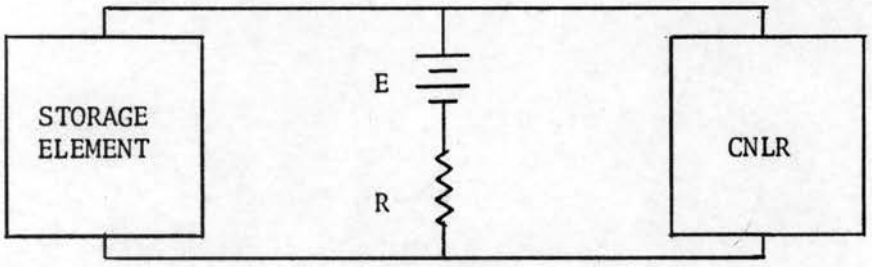


Figure 12. General CNLR Oscillator

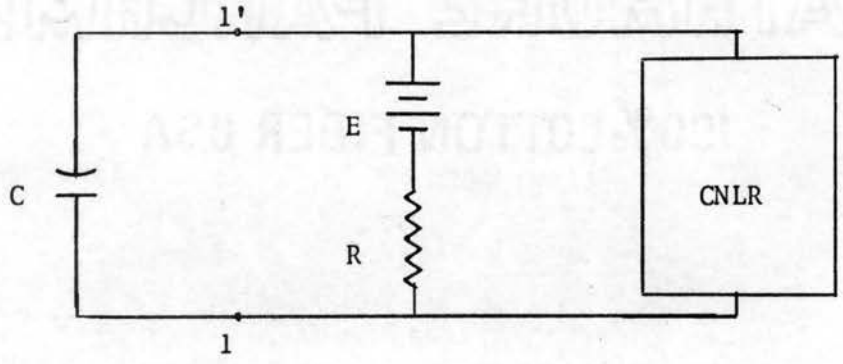


Figure 13. Basic CNLR Oscillator

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[2]Leonard Strauss, Wave Generation and Shaping, (York, Pennsylvania, 1960).

The effect of the capacitor on the stability criteria developed earlier is paramount. In fact, since the circuit in Figure 12 is no longer a series circuit, it is possible that the previously developed stability criteria no longer applies. This is indeed the case. The first step in analyzing the basic CNLR oscillator is then to determine the biasing requirements necessary for instability.

Consider the driving point impedance at terminals 1-1' of the basic CNLR oscillator circuit (Figure 13) with the capacitor disconnected. If the CNLR is replaced by its piecewise linear model in the negative resistance region, the Norton equivalent of the circuit is as shown in Figure 14.

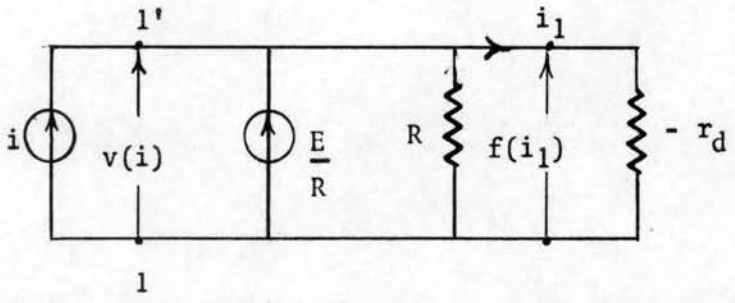

Figure 14. Norton Equivalent of Basic CNLR Oscillator Circuit Without Capacitor

The driving point impedance of this circuit is

$$R_{dp} = \frac{Rr_d}{r_d - R} \quad .$$

The only possibility for the driving point impedance to be negative is with $R > r_d$, where $r_d > 0$. As was to be expected, exactly the same criteria as was developed in Equation (2) for the series CNLR circuit applies in this case. Indeed, if this were not so, something would be seriously wrong; since the two circuits are identical as long as the

capacitor is not connected.

Starting with the generalized piecewise linear v-i characteristics of a CNLR device, as shown in Figure 9b, a first step in determining stability criteria of the basic CNLR oscillator circuit is to obtain the input characteristics at the terminals to which the capacitor is to be connected. The circuit to be analyzed is shown in Figure 14. $f(i_1)$ represents the functional relationship of the voltage across the CNLR to the current i_1. The characteristics of interest relate v and i.

The node equation governing the circuit is

$$i + \frac{E}{R} = \frac{f(i_1)}{R + i_1} \quad .$$

Solving for i gives

$$i = \frac{f(i_1) - E}{R} + i_1 \quad , \tag{3}$$

The general form of Equation 3 is

$$i = G\ [\ i_1, f(i_1)]$$

and the input characteristics can be expressed as

$$F\ [i, v(i)] = 0 \quad , \tag{4}$$

but an implicit functional relationship such as $v = g(i)$ may not always be permissible. Equation (4) represents a two parameter family of curves with E and R as parameters. The implicit relationship will not always be allowable since certain values of the parameters E and R may cause v to be a multivalued function of i. The circuit in Figure 14 may now be simplified to that in Figure 15.

The only admissible solution to the open circuit in Figure 15 is

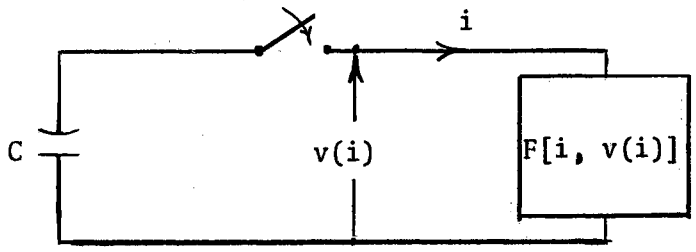

Figure 15. Basic CNLR Oscillator Circuit

with i = 0. Stable solutions of Equation (4) must therefore be points satisfying

$$F\ [o,\ v(o)] = 0 \quad .$$

The only possible solutions of Equation (4) which can be points of instability are those corresponding to intersections in the negative resistance region of the CNLR characteristics. Applying Equation (3) and noting that

$$v(i) = f(i_1) \quad ,$$

results in a simple linear transformation of the composite circuit of the CNLR and the bias network. Applying this graphical transformation to the CNLR characteristics and the two load line conditions indicated in Figure 16 results in the two curves in Figure 17.

Now, consider the circuit in Figure 15 where at some time t = 0, the switch is closed connecting the initially uncharged capacitor C across the network whose characteristics are given in Figure 17.

The loop equation governing this circuit is

$$-\frac{1}{C}\int i\ dt = e_C = v(i) \quad . \tag{5}$$

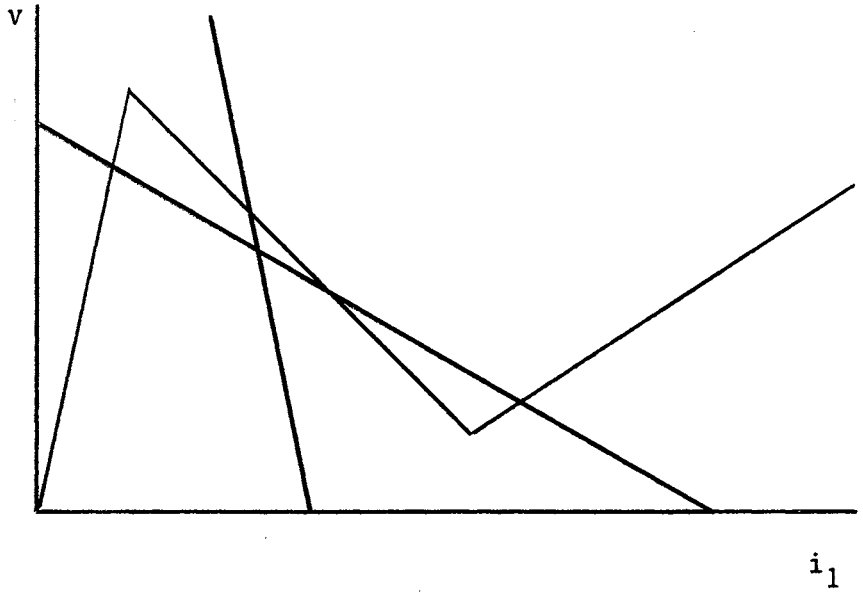

Figure 16. CNLR Circuit Characteristics Under Two Different Biasing Conditions Giving Intersections in the Negative Resistance Region

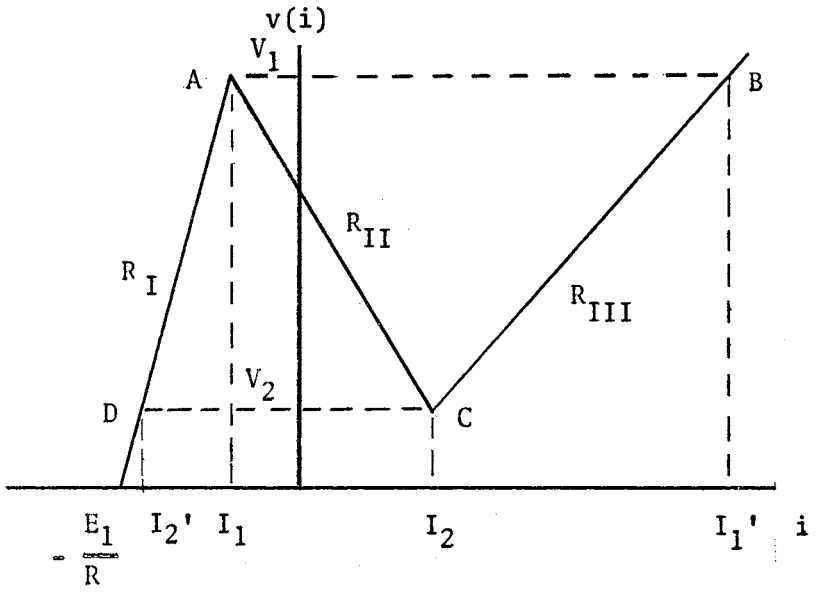

Figure 17. Input v-i Characteristics of Basic CNLR Oscillator Circuit Without Capacitor, $R > R_{II}$

The initial conditions governing the circuit are only that

$$e_C(o) = 0 \ .$$

Thus, since the voltage across the capacitor cannot change instantaneously, at $t = 0^+$ the circuit must be operating at the point

$$(v, i) = (0, -\frac{E}{R}) .$$

At $t = 0^-$, the circuit was operating at a stable point where $i = 0$, but no restrictions have been placed on the CNLR circuit so that instantaneous current and voltage jumps are allowable.

The negative current,

$$i = -\frac{E}{R}$$

flowing through the capacitor causes it to charge such that e_C increases. The charging rate is determined by the magnitude of C and the incremental resistance of the characteristic. As the capacitor voltage charges, i will decrease and eventually the capacitor voltage will reach the voltage V_1. A current I_1 will then be flowing through the capacitor requiring the capacitor to continue charging. The only possible way for the voltage to continue increasing is for operation to switch to another point on the characteristics with the same voltage. It is assumed that the current can switch instantaneously, therefore, the operating point will instantaneously jump to the point (V'_1, I'_1), where $V_1 = V'_1$.

Now, I_1 is positive and the capacitor must discharge, hence the operating point will follow the characteristics as v decreases toward zero. The voltage will decay expotentially with a time constant determined by C and R_{III}.

Upon reaching the voltage V_2, the only way that e_C can continue decreasing is to switch operating points to the point (V'_2, I'_2), which it instantaneously does. The current jumps from I_2 to I'_2 and, since

the current reverses its sign, the capacitor again begins to charge expotentially along the R_I characteristics. Upon reach the voltage V_1, the cycle will repeat itself along the path ABCDA.

If the other set of characteristics are considered, it is readily seen that the circuit will become stable when the voltage across the capacitor has charged to the value indicated at the intercept of the R_I characteristic and the i = 0 axis. In fact, since the sign of i determines the sign of the time derivative of the voltage across the capacitor, it is apparent that all current axis intercepts are stable points if the slope of the v-i characteristics at the intercept is positive. Conversely, if the slope of the v-i characteristics at the intercept is negative, then the intercept is a point of instability.

If the capacitor has some initial charge at the time it is switched into the circuit, independent of the charge, the locus of operation will eventually be exactly the same as the uncharged case. Thus, in this case, the mode of operation is independent of the initial conditions.

In addition to the linearization of the CNLR characteristics, it has been assumed that instantaneous current switching can take place. Each of these assumptions is an idealization which is seldom valid. As was mentioned earlier, the finite lead inductance and non-zero transient time of the CNLR device may cause the switching locus to be curved. This effect becomes more pronounced as the frequency of operation is increased, since inductive reactance increases with frequency and tends to oppose any change in current.[3] Also, if semiconductor devices are

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[3]H. J. Zimmermann and S. J. Mason, Electronic Circuit Theory (New York, 1959).

employed, the rather slow transition time inherent to semiconductor materials becomes a problem as the frequency increases.

Referring again to the astable oscillator characteristics, it is convenient to graphically determine the v-t and i-t waveforms. These are shown in Figure 18. Assuming zero transition time in the switching regions, the frequency and form of these oscillations can be accurately determined, subject to the error introduced by the piecewise linearization of the CNLR

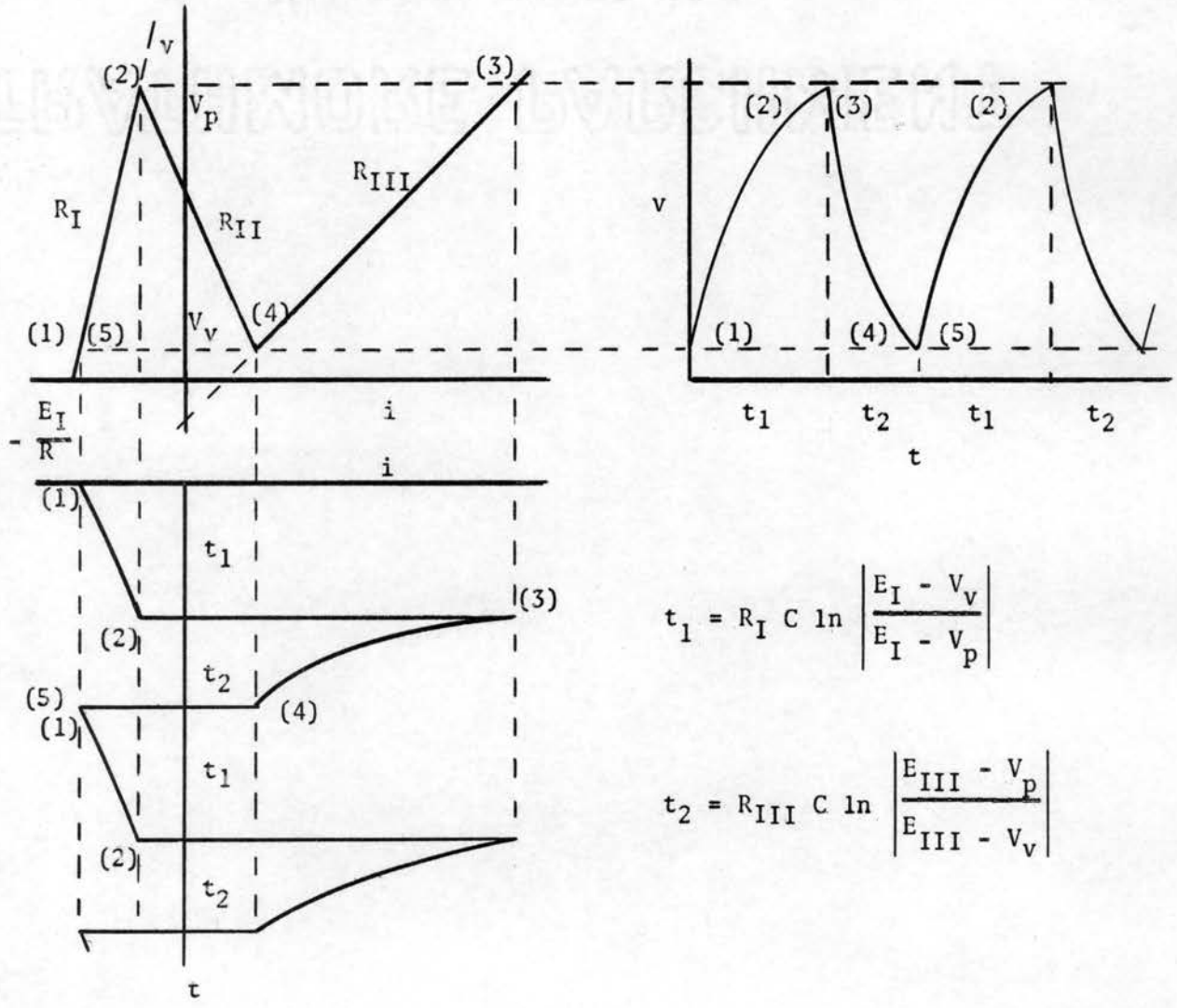

Figure 18. Astable CNLR Oscillator Waveforms--Idealized Case

The parameters presented in Figure 18 are defined as follows:

E - Bias voltage associated with the external resistance R

E_I - Open circuit voltage of piecewise linear model in state I

R_I - Thevinin equivalent resistance of state I

E_{III} - Open circuit voltage of piecewise linear model in state III

R_{III} - Thevinin equivalent resistance of state III

V_p - Peak voltage at which the CNLR device turns on

V_v - Valley voltage at which the CNLR device turns off.

Knowledge of the initial voltage, the final voltage, the voltage to which the capacitor is trying to charge, and the time constant are sufficient to determine the period of charge. V_p and V_v are device parameters. R_I and R_{III} are simply the parallel combination of R and the piecewise linear resistance of the model in the particular region under consideration. E_{III} is a function of the value of E, R_{III}, and the voltage associated with the piecewise linear model of the negative resistance region. E_I is dependent only upon E, R, and R_I.

Simplifying assumtpions can usually be made when the actual v-i characteristics of the CNLR device are available. For instance, some of the parameters associated with the four-layer diode are typically

$$V_p = 30 \text{ volts}, \quad V_v = 0.8 \text{ volts},$$

$$R_{\text{state I}} = 10^6, \text{ and } R_{\text{state III}} = 10^2 \text{ ohms}.$$

A typical value of bias resistor might be $R = 5 \times 10^4$ ohms. It is readily seen that little error is generated by taking

$$E_I \simeq E, \quad E_{III} \simeq 0, \quad R_I \simeq R,$$

$$R_{III} \simeq R_{\text{state III}}, \text{ and } V_v \simeq 0.$$

When the above approximations are substituted into the equations giving the time intervals in Figure 18, the following equations result:

$$t_1 = RC \ln\left|\frac{E}{E - V_p}\right|, \quad E > V_p$$
$$t_2 = R_3 C \ln\left|\frac{V_p}{V_v}\right| \tag{6}$$

V_v is usually so small that it is difficult to accurately measure, but the holding current of the four-layer diode is rather easy to measure. The discharge time of the capacitor is therefore best given as

$$t_2 = R_3 C \ln\left|\frac{V_p}{I_h R - E/R}\right| \tag{7}$$

Actually, little error is introduced if t_2 is taken as

$$t_2 \simeq 3.5 R_3 C ,$$

since usually $20 \leqslant \frac{V_p}{V_v} \leqslant 40$ for typical four-layer diodes.

Equation (6) indicates that the charging time can be varied radically by varying the bias voltage. Care must be taken in changing E, for the circuit must remain biased in the negative resistance region. Changing C changes t_1 and t_2 equally, but changing R changes only t_1. Again, the bias condition must not be upset.

It is possible that the peak value of current which flows through the CNLR when the device switches on will exceed the maximum current rating of the device. If this is the case, than a small resistance can be placed in series with the capacitor to limit this current to a safe value. The value of this limiting resistor R_L should be such that

$$\frac{V_p}{R_L} < I_{max} .$$

In most cases, the effect of this added resistance on t_1 will be negligible, although it may have a considerable effect on t_2.

Attention will now be directed to the case where the lead inductance and transient time of the CNLR device are considered. The effect of these transient phenomena is to give a decided curvature to the switching locus.[4] Figure 18 is reproduced in Figure 19 indicating the locus of operation for both cases.

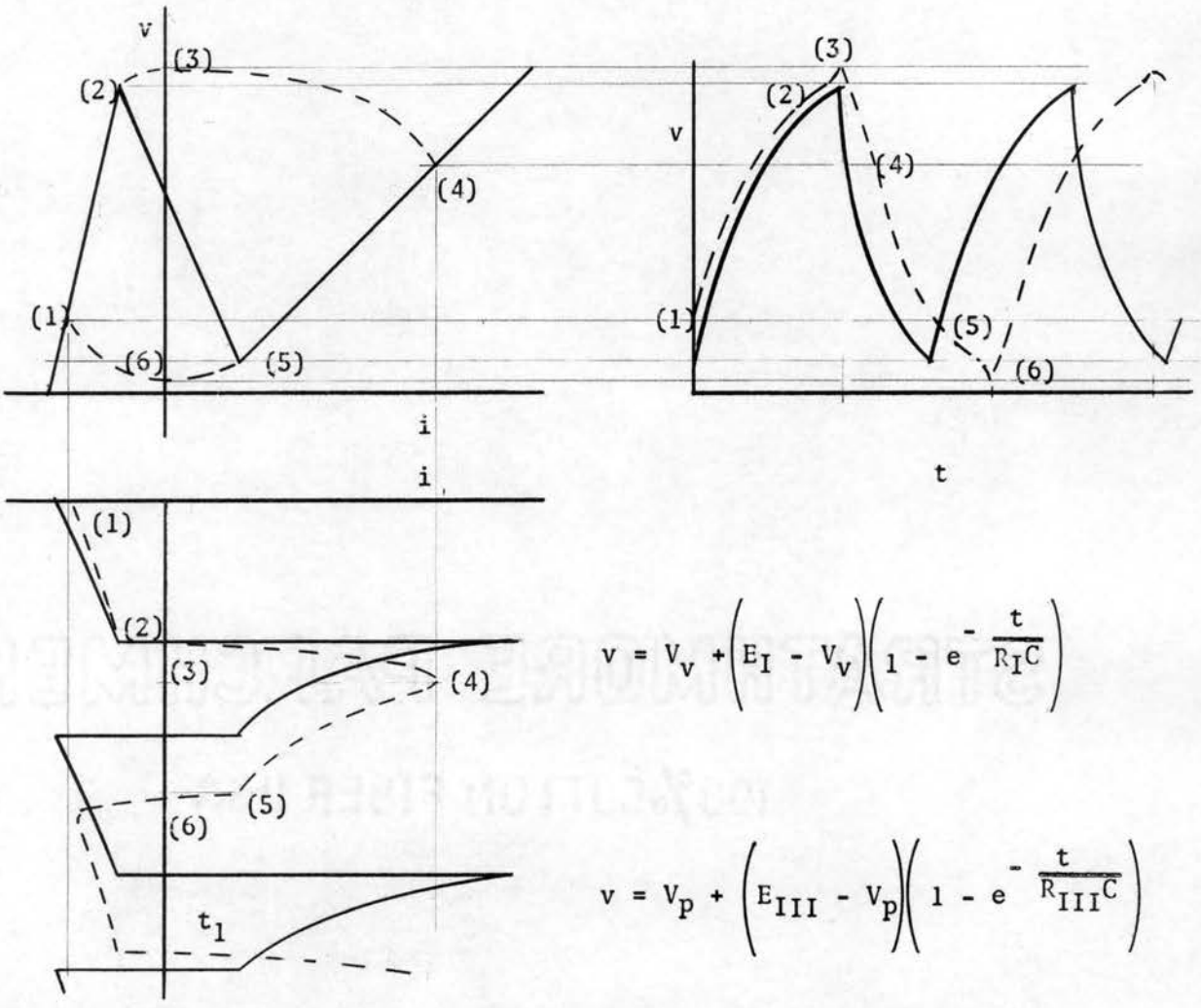

Figure 19. Basic CNLR Oscillator Characteristics--Transient Behavior

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[4] A. A. Andronow and C. E. Chaikin, Theory of Oscillations (Princeton, New Jersey, 1949).

It is noted that the curve of V versus t for $L \neq 0$ is quite similar to a sine wave.

Consider the circuit in Figure 20.

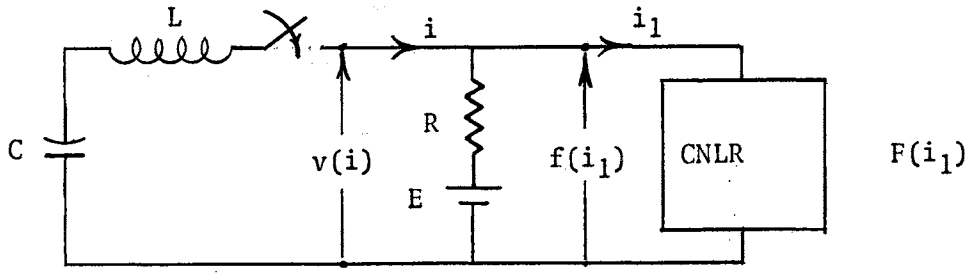

Figure 20. Basic CNLR Sinusoidal Oscillator

The addition of the second storage element renders the graphical method of analysis rather useless, so this circuit will be analyzed with the CNLR characteristics considered as being piecewise linear.

As before, the piecewise linear model of each of the piecewise linearized regions of the CNLR's characteristics are simply a resistance

$$r_k = \frac{v(i_1)}{i_1} ,$$

and a voltage source E_k. The Thevinin equivalent circuit of the resistance and sources in Figure 20 is given in Figure 21, where

$$R_t = \frac{Rr_k}{R + r_k}$$

and

$$E_t = \frac{Er_k + E_k R}{R + r_k}$$

Writing the single equation for the current in Figure 21 gives

$$E_t = - [i R_t + L \frac{di}{dt} + \frac{1}{c} \int i \, dt] \tag{8}$$

The auxiliary equation associated with Equation (8) is

$$R_t + L s + \frac{1}{cs} = 0 \tag{9}$$

where s is the Laplacian operator. Multiplication by $\frac{s}{L}$ gives

$$s^2 + \frac{R_t}{L} s + \frac{1}{Lc} = 0 \, . \tag{10}$$

Equation (10) has two roots given as

$$s = - \frac{R_t}{2L} \pm \sqrt{\frac{R_t}{2L}^2 - \frac{1}{Lc}} \tag{11}$$

or

$$s = \alpha \pm j \omega \, . \tag{12}$$

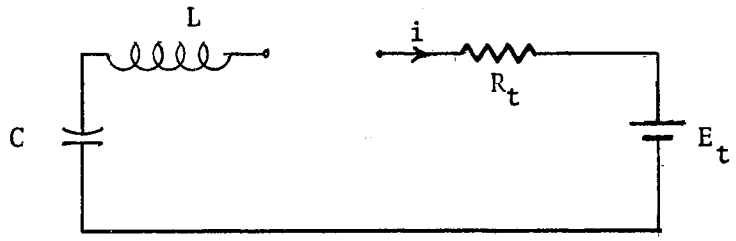

Figure 21. Thevinin Equivalent of Basic CNLR Oscillator Circuit

For a growing transient reponse, $\alpha > 0$. This requires that

$$\frac{R_t}{2L} < 0 \, .$$

Since L is positive, a necessary condition for a growing transient response is that

$$R_t < 0 \, . \tag{13}$$

The only possibility of Equation (13) being satisfied is for r_k to be negative and less in magnitude than R. Substituting for r_k in the negative resistance region,

$$r_k = - r \ , \ r > 0$$

gives

$$R_t = \frac{RL}{r - R} < 0 \tag{14}$$

which is true if and only if

$$R > r \ . \tag{15}$$

Of course, a growing transient cannot be exhibited indefinitely, since the circuits operation would eventaully reach a region where

$$r_k = \frac{\partial v(i_1)}{\partial i_1}$$

which would indicate a decaying transient.

For sinusoidal oscillations, ω must be real. This requires that

$$\frac{1}{LC} > \left(\frac{R_t}{2L}\right)^2 \ ,$$

or

$$R_t^2 - 4 \frac{L}{C} < 0 \tag{16}$$

Factoring the left hand side of Equation (16) gives

$$\left(R_t - 2\sqrt{\frac{L}{C}}\right)\left(R_t + 2\sqrt{\frac{L}{C}}\right) < 0 \tag{17}$$

Now $R_t < 0$, therefore, for Equation (17) to be satisfied, requires that

$$2\sqrt{\frac{L}{C}} > \left|R_t\right| \ . \tag{18}$$

The two requirements on the circuit in Figure 20 which are necessary for an increasing sinusoidal response may then be embodied in the single inequality

$$-2\sqrt{\frac{L}{C}} < R_t < 0 \qquad (19)$$

The parameters to which the designer has access are R, L, C, and E. The value of r is usually determined from an inspection of the CNLR's characteristics. The condition $R > r$ has been established, as well as a value of E such that the circuit is biased in the negative resistance region of the CNLR.

Equation (19) may be written

$$-a(r - a) > rR > 0$$

where

$$a = 2\sqrt{\frac{L}{C}} \quad , \text{ and } (r - R) < 0 \quad .$$

Then,

$$-ar + aR - rR > 0 > -rR \quad .$$

and

$$R(a - r) > ar > ar - rR \quad .$$

Now, if

$$(a - r) > 0 \quad ,$$

then

$$R > \frac{ar}{a - r} > \frac{r(a - R)}{a - r} \quad . \qquad (20)$$

The equation

$$R = \frac{ar}{a - r}$$

is a hyperbola in the r, R plane as shown in Figure 22. The restriction

$$0 < r < R$$

indicates that only the first quadrant of the r, R plane need be considered. The inequality

$$\frac{ar}{a - r} > \frac{ar}{a - r} - \frac{rR}{a - r}$$

in Equation (20) reduces to $R > r$. The equation R = r is a straight line with unity slope

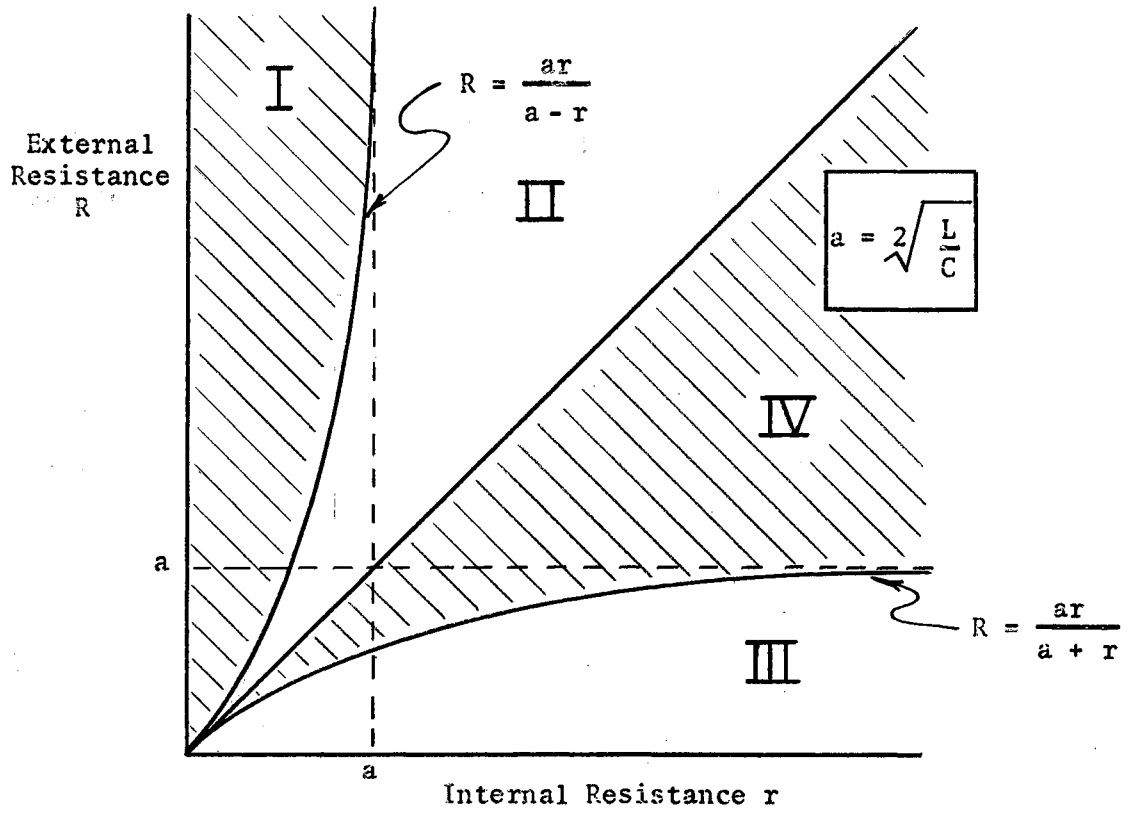

Figure 22. Modes of Operation of Basic CNLR Oscillator Circuit as a Function of Internal and External Resistance

Now $R > r$ implies that

$$\frac{a - R}{a - r} < 1 \quad .$$

Equation (20) is restricted to the range of r such that $0 < r < a$ and the domain of R,

$$R > \frac{ar}{a - r} > 0 \quad .$$

Thus, Equation (20) is satisfied by all points in region #1 (Figure 22). If $(a - r) < 0$, then

$$R < \frac{ar}{a - r} < \frac{r(a - R)}{a - r}$$

which implies that R is negative, which is not allowed. Thus, Region #1 is the only region in the first quadrant of the r, R plane which allows sustained sinusoidal oscillations.

It is of interest to note the other possibilities which arise as possible solutions of Equation (10). The inequalities

$$R > r \ , \alpha > 0$$

and

$$R_t^2 > 4 \frac{L}{C} \ , \ \omega \text{ real} \ ,$$

are satisfied in Region #2. This is easily shown since

$$\left(R_t - 2\sqrt{\frac{L}{C}}\right)\left(R_t + 2\sqrt{\frac{L}{C}}\right) > 0$$

requires that

$$- \left|R_t\right| + 2\sqrt{\frac{L}{C}} < 0$$

since $R_t < 0$. Thus,

$$R_t < -2\sqrt{\frac{L}{C}} < 0 \quad .$$

In the notation of Equation (20) this becomes

$$\frac{Rr}{r - R} < -a < 0 \quad ,$$

which gives

$$Rr > -a(r - R) > 0$$

or

$$0 > -ar + aR - rR > -rR \quad .$$

This reduces to

$$r(a - r) < R(a - r) < ar \tag{21}$$

Now in this case (a - r) must be positive to satisfy Equation (21), hence

$$R < \frac{ar}{a - r} \quad . \tag{22}$$

Region #2 is defined as the set of points in the first quadrant which satisfy

$$0 < r < R < \frac{ar}{a - r} \quad .$$

Sets of parameters which satisfy Region #2 indicated the circuit response will be in the form of relaxation oscillations.

In the case

$$R < r \ , \quad \alpha < 0$$

and

$$0 < R_t < 2\sqrt{\frac{L}{C}} \quad , \qquad \omega \text{ real} \ ,$$

R and r must satisfy

$$R < r \quad , \; a > \frac{rR}{r - R} > 0 \quad .$$

This can be written as

$$0 < R < \frac{ar}{a + r} < r \quad . \tag{23}$$

Region #3 consists of the set of points which satisfy Equation (23). The circuit response in this region is a damped sinusoidal oscillation.

If the conditions

$$R < r \; , \; \alpha < 0$$

$$R_t > 2\sqrt{\frac{L}{C}} \; , \; \omega \text{ real} \; ,$$

are satisfied, the circuit response will be damped expotential pulses. These conditions can be written as

$$R < r \; , \; \frac{rR}{r - R} > a > 0 \quad .$$

Solving for R gives

$$R > \frac{ar}{a + r} > 0 \quad .$$

Thus, Region #4 is obtained such that

$$R < r \; , \; R > \frac{ar}{a + r} > 0 \quad .$$

Subject to the accuracy of the piecewise linearization, it is then possible to obtain a particular oscillitory mode by adjustment of R, L, C, and the bias voltage. The ease in which sinusoidal oscillations may be obtained is enhanced by making Region #1 as large as possible.

This is done by increasing the ratio $\frac{L}{C}$. If $\frac{L}{C}$ is made quite small, it will become very difficult to obtain sinusoidal oscillations, since the inherent non-linearities of the CNLR will exhibit a greater influence. It should be noticed that when Region #1 is made larger, so is Region #4.

The solution of Equation (8) for the frequency of the sinusoidal oscillations gives

$$\omega = \frac{1}{\sqrt{LC}} \sqrt{1 - \frac{R_t^2 C}{4 L}} \quad .$$

If $\frac{R_t^2 C}{4 L}$ is made much less than unity, then to a first approximation,

$$\omega \simeq \frac{1}{\sqrt{LC}} \quad . \tag{24}$$

R_t^2 can be made small by keeping the value of (R - r) very small. $\frac{C}{L}$ can be made small by making $\sqrt{\frac{L}{C}}$ very large. Hence, operation very near to the R = r line (Figure 22), but still keeping $R > \frac{ar}{a - r}$ allows the frequency to be obtained from Equation (24).

CHAPTER III

FOUR-LAYER DIODE THEORY

In Chapter II, a generalized theory of oscillations relative to non-linear resistance devices was developed. The actual v-i characteristics of the non-linear device being considered were found to be extremely important relative to the application of this theory to a particular device. The remainder of this thesis will be concerned with the application of the theory developed in Chapter II to a particular negative resistance device.

The most interesting one-port negative resistance device is the four-layer semiconductor diode. This device belongs to the general class of CNLR devices, although its v-i characteristics present certain properties which are unique to the device.

In Chapter V, the general oscillator theory developed in Chapter II will be considered in its application to the v-i characteristics of the four-layer diode. The author feels that this study will be considerably more enlightening to the reader if the internal machanisms of the four-layer diode are discussed before an attempt is made to utilize its characteristics. The similarity between a four-layer diode and a pair of PN junction diodes implies that a knowledge of PN junction theory would be a necessary building block in formulating a complete analysis of the four-layer diode. For this reason, a brief treatment of the pertinent portions of PN junction theory is presented at this point.

A PN junction diode consists essentially of a tiny piece of P-type semiconductor material which is chemically bonded to a similar piece of N-type material. Various bonding techniques are used to form the junction between the two materials, the most common being that of adding certain impurities to intrinsic material in the melted stage. When the junction is formed, there is an immediate depletion of electrons and holes in the region near the actual junction due to their attraction into the opposite material. This depletion of free electrons and holes continues until a state of equilibrium exists with a voltage present across the junction. In this equilibrium condition, this barrier voltage is just large enough to prevent further diffusion of carriers across the depletion region.

The electric field present across the depletion region is analogous to the field produced by a space charge near the cathode of a vacuum tube. It is known that a finite number of electrons still leave the cathode, otherwise the space charge could not exist.

Figure 23 is a plot of barrier voltage versus depletion layer width from an idealized qualitative standpoint.

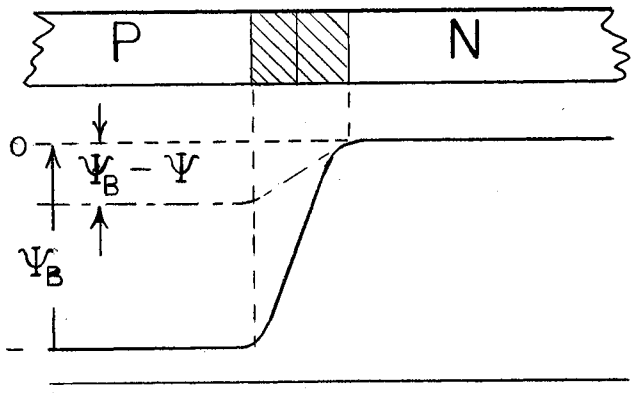

Figure 23. PN Junction Diode Barrier Voltage--Unbiased State

The actual thickness of the depletion region is quite dependent upon the degree of doping of each material, and extends further into the region of lighter doping.

If now, a forward bias voltage is applied to the diode as in Figure 24, it is seen that the barrier voltage across the junction is reduced to a value $\Psi_B - \Psi$ where Ψ_B is the open circuit barrier voltage and Ψ is the applied bias voltage. In this condition, many electrons will possess sufficient energy to cross this barrier from the N side to the P side, and similarly many holes in the P side will be able to cross into the N side. It is found that quite a large current now flows across the junction in the forward direction, i.e., from P to N. This condition--the forward biased state--is commonly referred to as the "saturation" or "on" state of the diode.

If, however, the junction is reversed biased by the addition of a voltage making the P side negative with respect to the N side, it is found that the barrier voltage is enhanced, resulting in even fewer carriers crossing the barrier. Thus, only a small current flows in the reverse biased or "off" state.

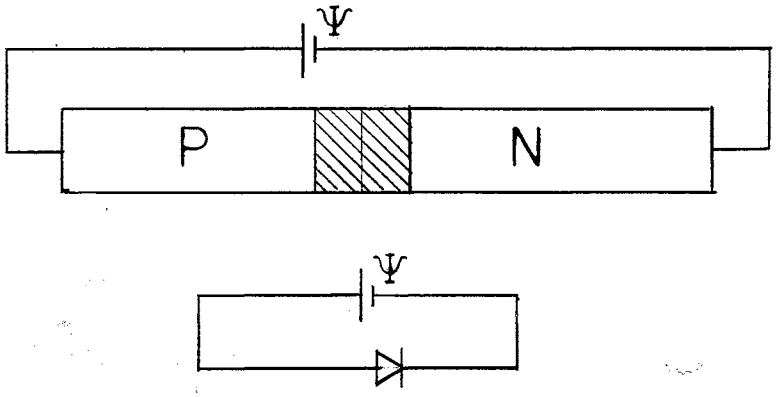

Figure 24. Forward Biased PN Junction Diode

Even though a material is said to be P type, there are some available electrons in the material, and similarly there are a few holes in N-type material. These carriers can easily cross the reversed biased junction and thus constitute a finite reverse bias current across the junction.

If the reverse bias voltage is made quite large, the diode may experience a form of breakdown and conduct very heavily in the reverse direction. There are at least three different mechanisms which can cause this breakdown. Avalanche breakdown[1] occurs when high velocity carriers collide with the crystal lattice structure so violently that some of the atoms in the lattice structure become ionized and release hole-electron pairs. These new charges, under the influence of the high electric field are accelerated and may cause further ionization of the lattice atoms. This effect may become cumulative and allow very high currents to flow.

Zener breakdown[2] occurs when the field across the junction becomes so intense that it actually pulls electrons and holes away from the atoms to which they are associated. This effect is very similar to high field emission in vacuum tubes.

Punchthrough[3] occurs mainly in transistors. As the voltage across a depletion region is increased in the reverse direction, the width of the depletion region increases. It is possible for this region to move

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[1]S. L. Miller, "Avalanche Breakdown in Germanium," Physical Review 99, August 15, 1955, p. 1234.

[2]L. P. Hunter, Handbook of Semiconductor Electronics (New York, 1956).

[3]Ibid.

entirely through the device, thus rendering its semiconducting properties useless.

The useful characteristics of the four-layer diode arise from avalanche breakdown; therefore, this phenomena shall be considered in some detail.

A reverse biased PN junction will have a finite value of current flowing across the junction. As the reverse bias is increased, the magnitude of this current approaches a constant value called the reverse saturation current, which is normally only a few microamps. As the reverse bias is further increased, the electric field present across the depletion region becomes more and more intense, and the carriers which do fall through this field are given more and more kinetic energy. When this field becomes intense enough, the carriers are imparted sufficient kinetic energy to actually break the covalent bonds of the stable atoms in the lattice structure. As a result, additional carriers are made available, thus increasing the reverse current and also increasing the probability of more collisions. In very abrupt junctions, this avalanche of current may occur very rapidly and result in a very large reverse current.

The ratio of the electrons collected in the N-type material to those emitted into the depletion region by the P-type material is defined as the multiplication factor for electrons, M_e. The multiplication factor for holes, M_h, is similarly defined. An empirical relationship relating the multiplication factor to the junction voltage is given in Equation (25).[4]

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[4]S. L. Miller, "Avalanche Breakdown in Germanium," Physical Review Volume 99, No. 4, August 15, 1955, p. 1234.

$$M(V) = \frac{1}{\left[1 - \left(\frac{V}{V_B}\right)^{\eta}\right]} \qquad (25)$$

η is a function of the resistivity and type of the high resistivity side of the junction. V_B in Equation (25) is defined as the Avalanche breakdown voltage. A plot of Equation (25) (Figure 25) indicates that M increases very rapidly as V approaches V_B.

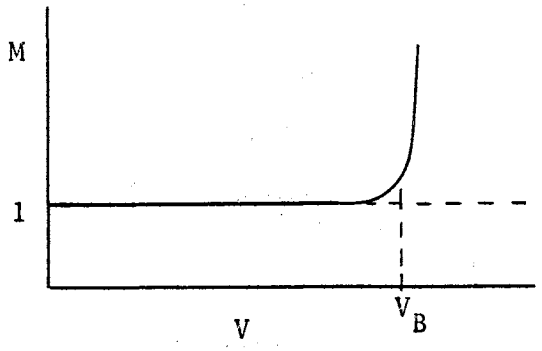

Figure 25. Multiplication Factor Versus Reverse Junction Voltage

Figure 26 shows a typical junction diode v-i characteristic. The current which flows after avalanche has taken place must be limited by the external circuitry.

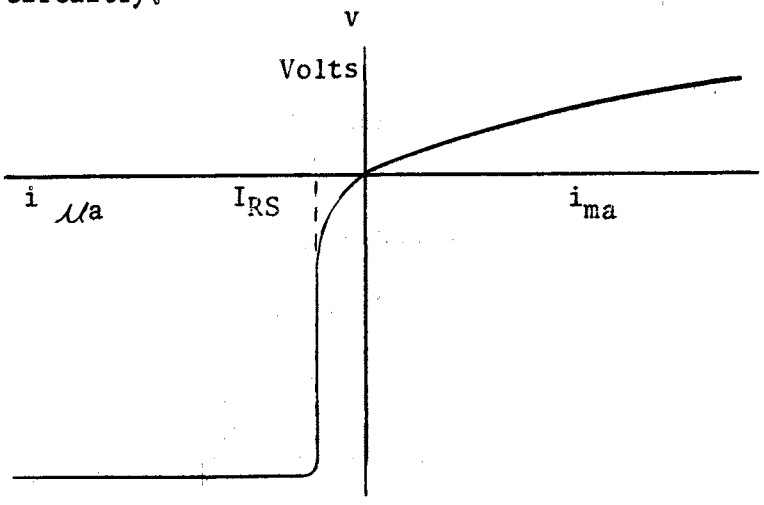

Figure 26. V-I Characteristics of Junction Diode

The junction transistor consists of three alternate layers of P and N materials and, therefore, has two junctions. When a PNP transistor is formed, initially, holes diffuse from the P regions into the base N region. As in the case of the junction diode, a state of equilibrium is finally reached with the establishment of barrier potentials across each of the two junctions. The potential distribution across the PNP transistor is shown in Figure 27.

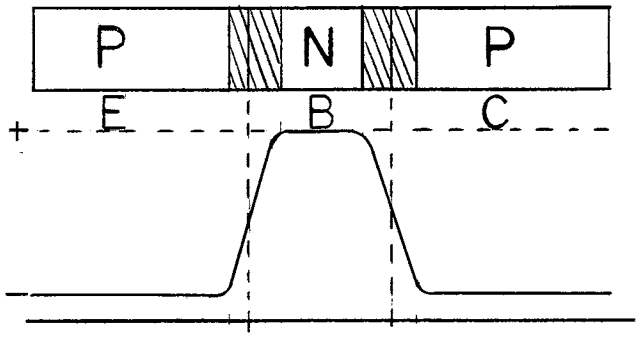

Figure 27. Potential Distribution--Unbiased PNP Transistor

As was indicated earlier, the width of an unbiased junction is primarily determined by the relative doping of the two adjacent regions. In actual practice, for reasons that will become evident in further development, the two P regions are doped much more heavily than the N region. The depletion layer of each junction therefore extends almost entirely into the N region.

It might be well to summarize the prevailing conditions in the various regions of the unbiased PNP transistor.

1. One of the P regions, called the emitter, and the other P region, called the collector, have an abundance of excess holes which are free to move under an applied electric field, but very few of the holes possess enough energy to surmount the barrier voltage separating

them from the N-type material.

2. The N-type material, called the base, has an excess of electrons, but most of them do not possess enough energy to surmount the emitter-base and collector-base barriers.

3. Two rather carrier free regions exist between the emitter and base and between the collector and base. Barrier voltages exist across these regions which oppose carrier flow between the emitter, base, and collector regions.

If now a small forward bias voltage is applied across the emitter and base terminals, as in the case of a forward biased junction, the emitter-base barrier will be lowered and will allow some of the higher energy holes in the emitter region to diffuse into the base. Similarly, higher energy electrons in the base will diffuse into the emitter.

If a reverse bias is now applied across the collector-base terminals, it would seem logical that a current similar to the reverse saturation current of a reverse biased junction diode would flow from base to collector. This voltage would increase the base-collector barrier so that holes in the base region near the base-collector junction might be swept into the depletion region and thus collected in the collector. Similarly, electrons in the collector region near the depletion layer might also be swept into the base. The sum of these hole and electron currents would compose the reverse current flowing from base to collector. Figure 28 shows the potential distribution across the PNP junction transistor with the emitter-base junction forward biased and the base-collector junction reverse biased.

The current flowing across the emitter-base junction is composed primarily of hole current, since the emitter is doped much more heavily

than the base. Only a small fraction of the total emitter current is due to electrons moving from the base into the emitter. These electrons contribute to positive current flow from emitter to base. The ratio of emitter hole current to total emitter current is called the emitter efficiency and is

$$\gamma = \frac{I_{eh}}{I_e} .$$

γ is usually only slightly less than unity.

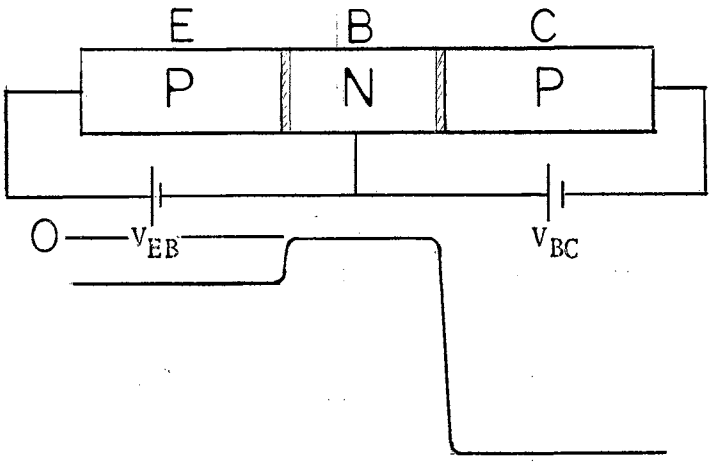

Figure 28. Potential Distribution--Normally Biased PNP Transistor

The emitter hole current

$$I_{eh} = \gamma \, I_e$$

is then injected into the base region. Some fraction of this hole current may diffuse far enough into the base region to come into contact with the electric field across the base-collector junction and thus be swept into the collector. The fraction of injected emitter hole current which is collected by the collector is given by

$$\beta_t = \frac{I_{ch}}{I_{eh}}$$

and is called the transport factor. The small fraction of hole current which is not collected is lost either by recombination in the base with ionized atoms or by falling back into the emitter. By making the base region very thin, the transport factor is made to approach unity, since this decreases the possibility of recombination in the base.

The holes which are swept into the collector attain a high kinetic energy as they pass through the collector barrier voltage, and as a result may, in their collisions with the lattice structure of the collector, create hole-electron pairs which tend to increase the collector current. The ratio of total collector current to collector hole current is given by

$$\delta = \frac{I_c}{I_{ch}}$$

and is called the collector efficiency.

In addition to the collector hole current, the normal reverse bias current I_{co} flows across the collector-base junction. I_{co} is defined as the collector current with the emitter current equal to zero and the base-collector junction reverse biased.

Neglecting I_{co}, the total collector current is seen to be

$$I_c = \delta \beta_t \gamma I_e = \alpha I_e$$

where

$$\alpha = \delta \beta_t \gamma = \frac{I_c}{I_e}$$

is the d-c current amplification factor from emitter to collector.

By controlled processes, α can be made to approach unity, hence

the collector current is approximately equal to the emitter current. The emitter current flows in a very low impedance forward biased diode circuit while the collector current flows in a high impedance reverse biased diode circuit. Thus, both a voltage and a power gain are possible between the emitter and collector terminals.

An NPN transistor can be analyzed in the same manner with the role of the electrons and holes being interchanged.

Before proceeding with the analysis of the four-layer diode, it might be profitable to look at its v-i characteristics. A schematic diagram of a four-layer diode and its characteristics are shown in Figure 29.

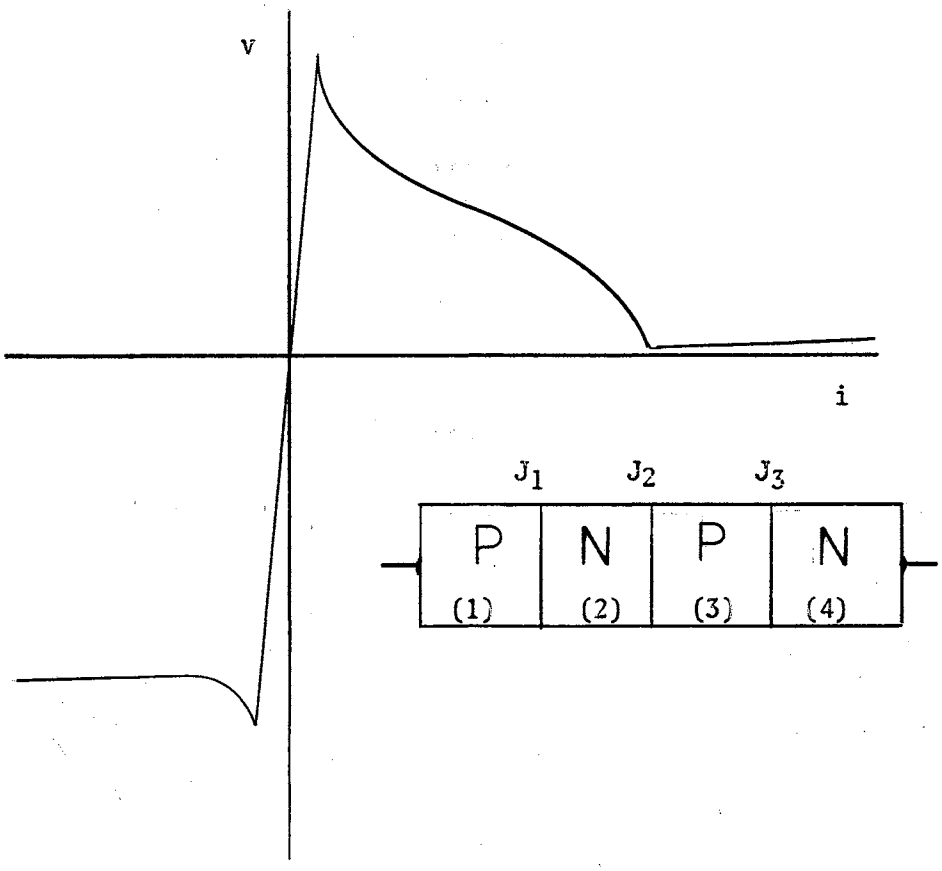

Figure 29. V-I Characteristics of Four-Layer Diode

When the four-layer diode is forward biased, junctions J_1 and J_3 are forward biased while the middle junction J_2 is reverse biased. For low forward bias voltages, the only current which can flow in the circuit is the normal reverse saturation current limited by the reverse biased junction J_2. In this condition, it may be assumed that the total terminal voltage is dropped across the reverse biased junction, since the ohmic drop in the bulk material and the drop across the forward biased junctions is negligible.

The total current passing across the junction J_2 is composed of that fraction of the holes which have been injected into region 2 from region 1 and collected by region 3, that fraction of the electrons injected by region 4 into region 3 and collected by region 2, and the normal reverse saturation current due to the flow of holes in region 2 into region 3 and electrons from region 3 into region 2. Thus, the total current across J_2 is

$$I_{(J_2)} = M_p \alpha_{1p} I + M_n \alpha_{2n} I + I_{co} \tag{26}$$

where

M_p = multiplication factor for holes across J_2

α_{1p} = normal current multiplication factor for the embodied PNP transistor

α_{2n} = normal current multiplication factor for the embodied NPN transistor

M_n = multiplication factor for electrons across J_2

Solving Equation (26) for I gives

$$I_{(J_2)} = \frac{I_{co}}{(1 - M_p \alpha_{1p} + M_n \alpha_{2n})} \tag{27}$$

Equation (27) may be considered as the fundamental equation governing the operation of a four-layer diode.

From transistor theory, it is known that the α of a transistor is a function of the emitter current (Figure 30). For low values of emitter current then,

$$\alpha_{1p} \ll 1 \quad \text{and} \quad \alpha_{2n} \ll 1$$

For low voltages, Figure 25 indicates that

$$M_p \simeq 1 \text{ , and } M_n \simeq 1 \text{ .}$$

Therefore, when $V < V_B$,

$$M_p \alpha_{1p} + M_n \alpha_{2n} \simeq \alpha_{1p} + \alpha_{2m} \ll 1$$

and

$$I \simeq I_{co} \text{ .}$$

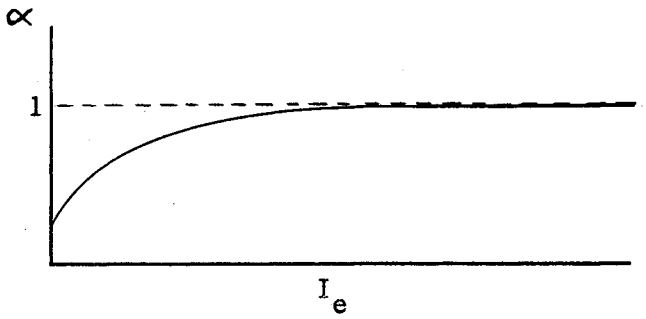

Figure 30. Transistor α Versue Emitter Current[5]

As the voltage across the four-layer diode is increased, the region where one of the M's in Equation (27) increases rapidly with V is reached. The denominator of Equation (27) then rapidly approaches zero,

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[5]L. P. Hunter, Handbook of Semiconductor Electronics (New York, 1956).

allowing the total current through the device to increase. This increase in current is due directly to avalanche multiplication across junction J_2.

If the value of

$$M_p \alpha_{1p} + M_n \alpha_{2n}$$

should become greater than unity, the current across J_2 would be greater than the total current through the device. Hence the voltage across J_2 must decrease, thus reducing M_p and M_n so as to keep the denominator of Equation (27) less than zero. Hence, a smaller voltage is required to keep the same value of current flowing. This indicates the presence of an incremental negative resistance region. For convenience, an expanded plot of the forward v-i characteristics of Figure 29 is shown in Figure 31.

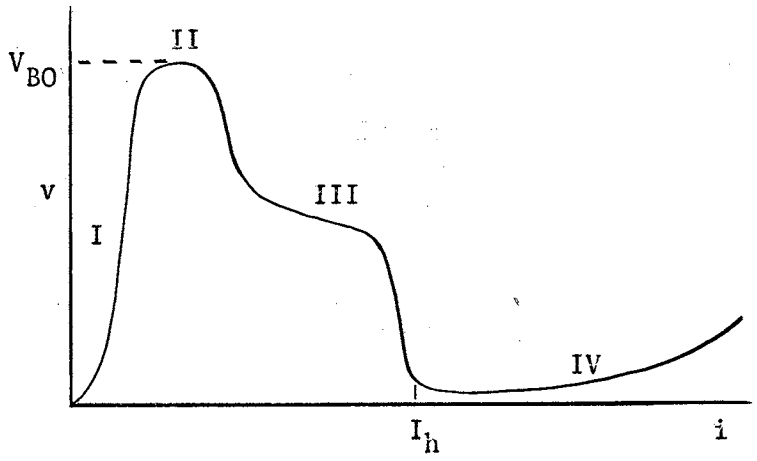


Figure 31. Idealized Forward V-I Characteristics of Four-Layer Diode

Calling

$$M_p \alpha_{1p} + M_n \alpha_{2n} = \alpha_t$$

is is seen that when V reaches V_{BO}, that α_t reaches 1 by the mechanism

of avalanche multiplication.

As soon as the current starts to increase (Region II), α_{1p} and α_{2n} increase due to increased current flow, and the amount of avalanche multiplication required to keep α_t near unity decreases. When the current becomes so large that $\alpha_{1p} + \alpha_{2n} = 1$, then the P_2 region must begin to emit holes into the N_1 region so as to keep the total current flow across J_2 from exceeding the total current flow through the device. Junction J_2 then must become forward biased. When J_2 becomes forward biased, the device takes on the characteristics of a single forward biased PN junction diode and will pass a very high current with only a very small voltage across the device.

For currents less than the value of current which flows when $V = V_{BO}$, the characteristics of the device are virtually voltage controlled. As soon as the voltage reaches V_{BO}, the characteristics become virtually current controlled. The three distinct regions of differential negative resistance (Region III) are not distinguishable in every device. It is believed that they are due to the fact that the junction J_2 is non-uniform and does not experience complete breakdown uniformly. By making J_2 extremely thin, it is found that the device experiences complete breakdown at a very low value of current.

The current at which breakdown is complete is called the holding current for the device. The devices which were available for this investigation were rated at a holding current of approximately 5 ma. One device, the junction of which was formed by an expitaxial firm process, was found which had a holding current of only 0.16 ma. The epitaxial firm process allows the junction to be virtually molecular in thickness, and it appears to experience complete breakdown uniformly.

Typical rated values for V_{BO} are from 25 to 35 volts, however, the device formed by epitaxial process broke down at approximately 23 volts.

As is the case with most semiconductor devices, the characteristics of the four-layer diode are extremely temperature sensitive. As the temperature of the device increases, avalanche multiplication may occur at lower values of terminal voltage. This is primarily due to the increase in the number of carriers which have sufficient energy to ionize atoms in the lattice structure after falling through the J_2 depletion region.

Typical values of "off" resistance (Region I) range from 100k ohms to 100 megohms, while the "on" resistance (Region IV) may be only a few ohms to 100 ohms. It is readily seen that the four-layer diode has extremely good possibilities as an imperfect switch, since it is essentially an open circuit in Region I and a short circuit in Region IV.

CHAPTER IV

APPLICATION OF TWO-PORT OSCILLATOR THEORY TO FOUR-LAYER DIODES

Chapter II dealt with general negative resistance characteristics and specifically with the piecewise linearized representation of the v-i characteristics of the CNLR type device. In this chapter, the methods used in Chapter II will be examined as to their application to the four-layer diode characteristics. The stability criteria developed in Chapter II was dependent only upon the slope of the v-i characteristics in a region and the associated circuit parameters. Hence, it should be expected that this same criteria would apply to similar regions of any exotic v-i configuration, assuming the voltage is a single valued function of the current. It is found that this criteria does apply in the case of the four-layer diode and indeed to any CNLR.

The v-i characteristics of a four-layer diode are reproduced in Figure 32.

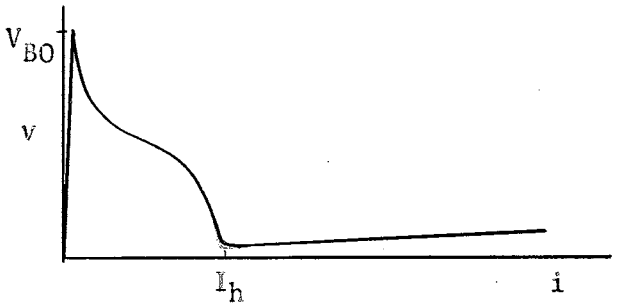


Figure 32. V-I Characteristics of Four-Layer Diode

For operation starting at i = 0, v = 0, the current is negligible for $0 < v < V_{BO}$, where V_{BO} is the break over voltage indicating the beginning of avalanche multiplication. For $i > I_h$, $v \simeq iR_{III}$, where I_h is defined as the holding current of the device.

Consider the series circuit in Figure 33, where the symbol represents a four-layer diode, and f(i) represents the terminal voltage across the diode as a function of diode current.

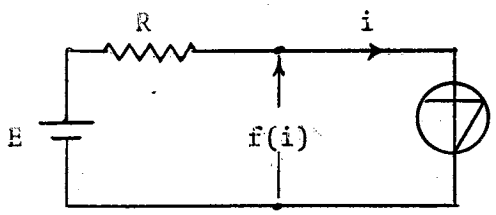


Figure 33. Series Four-Layer Diode Circuit

The equation representing the circuit is

$$E - iR - f(i) = 0 \ . \tag{28}$$

A set of solutions to this equation are the intersections of the current axis and the curve

$$\Psi(i) = E - iR - f(i)$$

which is plotted in Figure 34. Note that this particular curve is only one of a two parameter family of curves which can be obtained by using various values of E and R. In this particular case, the condition

$$I_h R < E < V_{BO}$$

is satisfied in addition to the fact that R is such that the load line

representation of E and R intersects the four-layer diode v-i characteristics the maximum number of times, this being five.

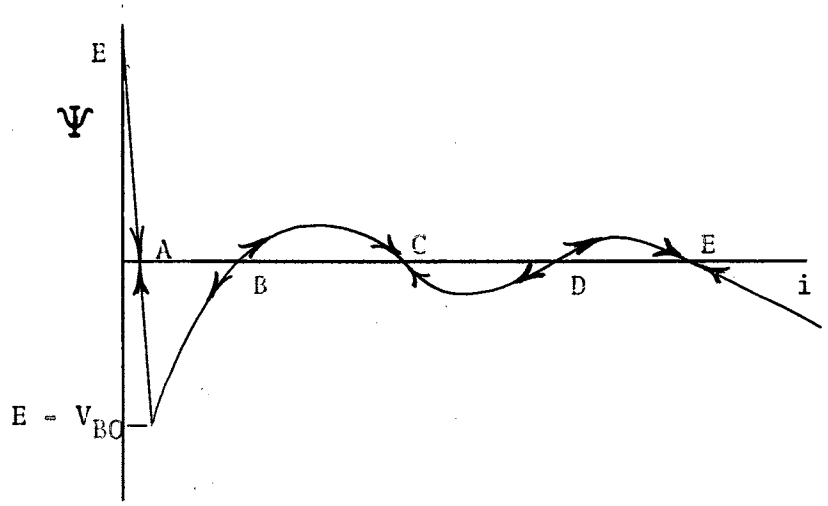


Figure 34. Graphical Solution of Equation 28

Considering operation at any of the solution points, it is seen that a perturbation of the current in the series circuit would immediately require a perturbation in the same direction for operation at points B and D, and a perturbation in the opposite direction for points A, C, and E. Hence, points A, C, and E are stable solutions and points B and D are unstable solutions. These conclusions are exactly as the analysis of the CNLR series circuit in Chapter II would dictate. This indicates that operation in the negative resistance region is stable if

$$\frac{\partial \Psi(i)}{\partial i} < 0$$

at the solution point.

Performing the differentiation on $\Psi(i)$ gives

$$\frac{\partial \Psi}{\partial i} = \frac{\partial}{\partial i}\left(E - iR - f(i) \right) = - \left(R + \frac{\partial f(i)}{\partial i} \right) < 0$$

for

$$R > \left| \frac{\partial f(i)}{\partial i} \right|$$

where

$$\frac{\partial f(i)}{\partial i} \leqslant 0 \quad .$$

The points of $\Psi(i)$ where

$$\frac{\partial \Psi(i)}{\partial i} = 0$$

must be considered as unstable solutions if they are indeed solution points of $\Psi(i) = 0$.

The application of the four-layer diode in the basic CNLR relaxation oscillator circuit is straightforward (Figure 35).

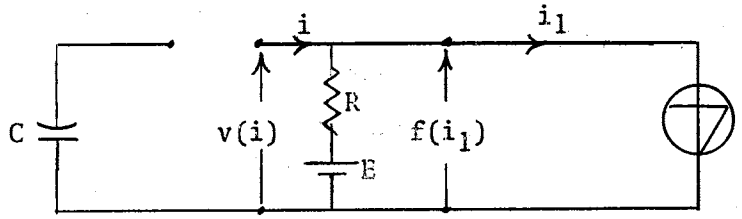


Figure 35. Basic CNLR Oscillator Circuit with Four-Layer Diode

The equations to be satisfied are

$$i = \frac{E}{R} + i_1 + \frac{f(i_1)}{R} \tag{29}$$

and

$$v(i) = -\frac{1}{C} \int i\,dt = f(i_1) \quad . \tag{30}$$

The graphical solution to Equation (29) with

$$v(i) = f(i_1)$$

is given in Figure 36 for the same E and R as in Figure 34.

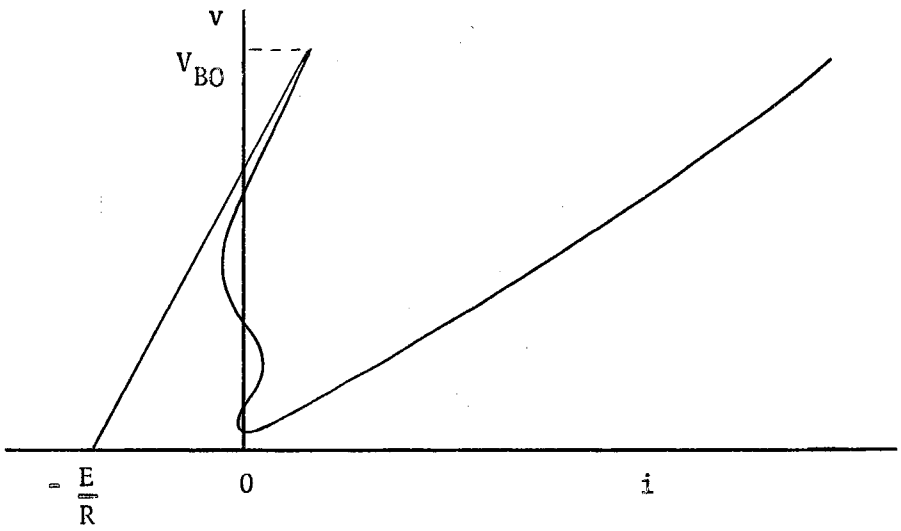


Figure 36. Graphical Solution to Equation 29

Rewriting Equation (29) as

$$i_1 = i + \frac{E}{R} - \frac{f(i_1)}{R}$$

and differentiating with respect to i gives

$$\frac{di_1}{di} = 1 - \left(\frac{df}{di_1}\right)\left(\frac{di_1}{di}\right)\frac{1}{R}$$

or

$$\frac{di_1}{di} = \frac{1}{1 + \left(\frac{df}{di_1}\right)\frac{1}{R}}$$

But

$$\frac{dv}{di} = \frac{df}{di} = \frac{df}{di_1}\frac{di_1}{di} \quad .$$

Thus,

$$\frac{dv}{di} = \frac{\frac{df}{di_1}}{1 + \frac{df}{di_1}\frac{1}{R}} \quad .$$

If $\frac{df}{di_1} \geqslant 0$, then $\frac{dv}{di} \geqslant 0$ and hence, the slope of the v-i curve is non-negative. If

$$\frac{df}{di_1} < 0 \quad \text{and} \quad \left|\frac{df}{di_1}\right| > R \ ,$$

then $\frac{dv}{di} > 0$. If

$$\frac{df}{di_1} < 0 \quad \text{and} \quad \left|\frac{df}{di_1}\right| = R \ ,$$

then

$$\frac{dv}{di} = \pm \infty$$

indicating the tangent to the v-i curve is vertical. These conditions are tabulated in Figure 37.

$\frac{df(i_1)}{di_1}$	$R + \frac{df(i_1)}{di_1}$	$\frac{dv(i)}{di}$
+	+	+
-	-	+
-	+	-
-	0	$\pm \infty$

Figure 37. Relationship Between $\frac{df(i_1)}{di_1}$ and $\left(\frac{dv(i)}{di} + R\right)$

Now, consider an equilibrium point of the v-i characteristics. Then $i = 0$, since if $i \neq 0$, the capacitor must be charging, indicating that the circuit is not in equilibrium. Let i be perturbed positively by an amount $\triangle i$. Then $i > 0$ and the capacitor voltage must decrease. However, if

$$\frac{dv}{di} > 0$$

at this point, then v cannot decrease; hence the current must decrease back to zero indicating that the equilibrium point was a stable point. On the other hand, if

$$\frac{dv}{di} < 0 \ ,$$

the capacitor voltage will decrease and i will increase further. In this case, operation will rapidly move away from the equilibrium point indicating that it was an unstable equilibrium point.

This shows that all stable equilibrium points must be in a region where

$$\frac{dv}{di} > 0 \ ,$$

conversely, all unstable equilibrium points must be in a region where

$$\frac{df}{di_1} \quad 0 \ ,$$

i.e., where

$$\frac{df}{di_1} < 0 \ , \quad \left|\frac{df}{di_1}\right| < R \ .$$

Continuous oscillations of any type cannot be sustained if the circuit has any stable equilibrium points. Thus, for sustained oscillations, the load resistance R and bias supply E must be such that

the v-i characteristics intersect the i = 0 axis only at points where

$$\frac{dv}{di} < 0 \quad .$$

An example of the resulting v-i characteristics which are a necessary condition for the existence of sustained oscillations with this circuit is shown in Figure 38.

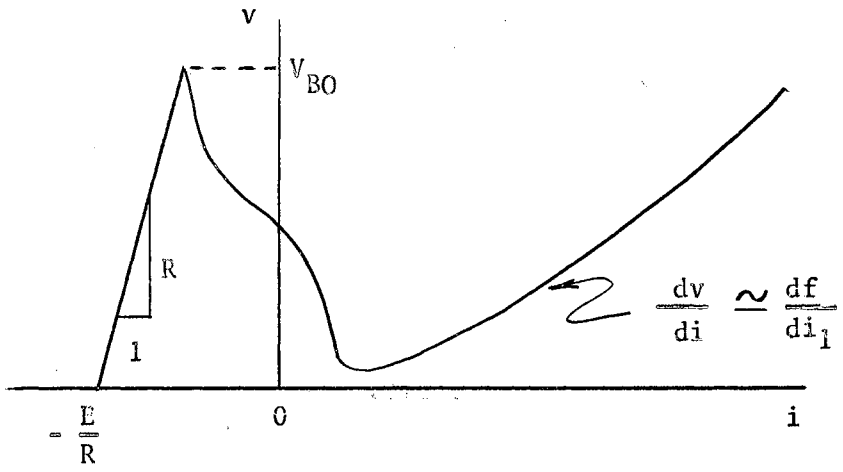


Figure 38. V-I Characteristics Necessary for Sustained Oscillations With Basic CNLR Oscillator Circuit Using Four-Layer Diode

It is noted that if

$$0 < \frac{df}{di_1} \ll R \quad ,$$

as is the case when the device is in the "on" condition, then

$$\frac{dv}{di} \simeq \frac{df}{di_1} \quad .$$

Similarly, when

$$0 < R \ll \frac{df}{di_1}$$

it is seen that

$$\frac{dv}{di} \simeq R \quad .$$

These two facts are great aids to quick sketching of the v-i characteristic, since normally these inequalities are satisfied in the "on" and "off" regions of the devices' characteristic. It should be noted that a necessary condition on E and R for sustained oscillations is that

$$V_{BO} < E < I_h R + V_h \tag{31}$$

where V_h is defined as the voltage across the device at $i = I_h$.

Since the value of I_h may not be as distinct as that of V_{BO}, the inequality

$$E < I_h R + V_h$$

should be treated conservatively. Since V_h is relatively small, in the magnitude of less than 1 volt, it should be sufficiently conservative to take

$$V_{BO} < E < I_h R \tag{32}$$

as a necessary condition for sustained oscillations. The conditions imposed on E and R in Equation (32) must be met if self oscillations are to be maintained, independent of the mode of oscillations.

Utilizing the methods of Chapter II, if the value of R is taken such that $R > r_m$; where

$$r_m = \max \left\{ \frac{\partial f(i_1)}{\partial i_1} \right\} \quad \text{and} \quad \frac{\partial f(i_1)}{\partial i_1} < 0 \ , \tag{33}$$

then the condition for an increasing transient response should be satisfied. If, in addition, the inequality

$$R > \frac{ar_m}{a - r_m}$$

is satisfied, then the operation corresponding to that in Region #1 (Figure 22) should be obtained. Similarly, decreasing

$$\sqrt{\frac{L}{C}}$$

such that

$$R < \frac{ar_m}{a - r_m}$$

would allow relaxation oscillations to be obtained.

It has been noted that the "off" resistance R_{off} of the four-layer is very large, while the "on" resistance R_{on} is very small. If $R \ll R_{off}$, then to a first approximation, the charging time of the relaxation oscillator with $L \simeq 0$ is given by

$$t_c \simeq RC \ln \left| \frac{E}{E - V_{BO}} \right| . \tag{34}$$

Equation (34) comes directly from Equation (7). Also since $R_{on} \ll R$, the discharge time is given by

$$t_d \simeq R_{on} C \ln \left| \frac{V_{BO}}{V_h} \right| . \tag{35}$$

In most cases,

$$V_{BO} = 25\ V_h \text{ to } 35\ V_h ,$$

therefore, to a fairly good approximation,

$$t_d \simeq 3.4\ R_{on} C . \tag{36}$$

The values of R_{off}, R_{on}, as well as that of r_m can be obtained

easily with a suitable transistor curve tracer, or statically from a point-by-point plot of the four-layer diode's static characteristics.

The value of the bias voltage is extremely critical as to the mode of oscillation. If $R > r_m$, then a very large range of E will still allow the circuit to be biased such that a growing transient can result.

CHAPTER V

EXPERIMENTAL RESULTS

In Chapter IV, a general one-port oscillator theory was examined in view of its application to the four-layer diode from a theoretical aspect. This chapter will be concerned with experimental measurements which were made in an attempt to verify the pertinent points of Chapter IV.

The experimental work performed in association with this thesis will be considered in the following sequence: First, the v-i characteristics of two four-layer diodes will be obtained and from them the applicable device parameters will be determined. Secondly, a relaxation oscillator will be constructed using, as a preliminary design, the device parameters in conjunction with the theory developed in Chapter IV. The agreement with, and/or deviations from, the expected results will then be compared. Third, a sinusoidal oscillator will be constructed, again using as a preliminary design, the device parameters and the theory from Chapter IV.

The two-layer diodes selected were of the same type, but exhibited quite different characteristics. The v-i characteristics of these devices were obtained from the visual presentation of a Type 575 Tektronix Transistor Curve Tracer. Figure 39 shows a simplified model of the curve tracer test circuit.

The magnitude of the maximum incremental negative resistance r_m

could not be determined accurately with the Type 575 Curve Tracer. The reason for this was that the maximum value of load resistance R_L (Figure 39) was 100k ohms, and this value was less than r_m for both devices. As an illustration of the effect of different values of R_L, consider Figure 40. Recalling from Chapter II that the series resistance and CNLR circuit is stable in the negative resistance region when

$$R > \frac{dv}{di} \quad ,$$

it is readily apparent that the entire v-i characteristic cannot be viewed unless R_L is greater than r_m. The value of r_m for unit #1 was only slightly greater than 100k ohms (Figure 40), while that of unit #2 was considerably larger than 100k ohms.

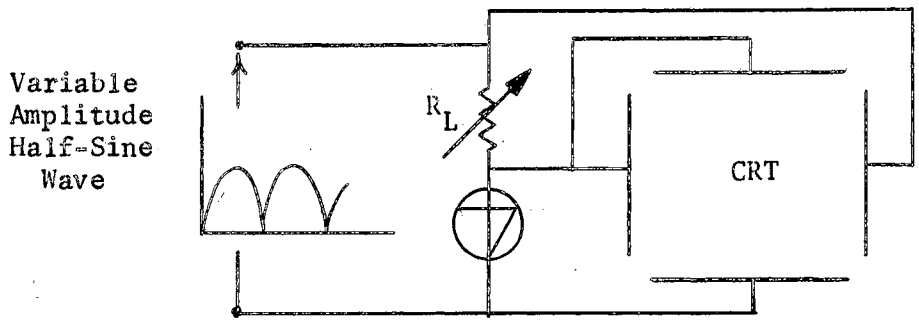


Figure 39. Simplified Model of Curve Tracer Circuit

A lower limit for r_m for unit #2 was determined by finding the magnitude of the ratio

$$\left| \frac{V_{BO} - V_h}{I_{BO} - I_h} \right| \quad .$$

This is the magnitude of the slope of the AA' line in Figure 40e.

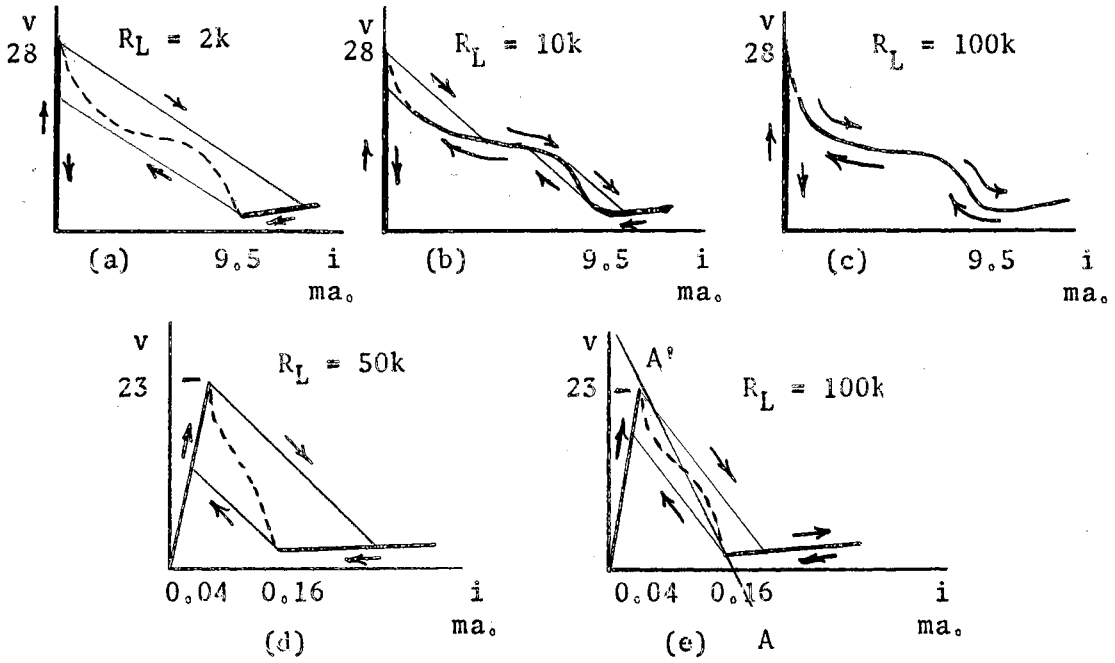


Figure 40. Curve Tracer Presentation as a Function of R_L

For unit #2 this value was approximately

$$\left|\frac{24 - 1}{0.04 - 0.16}\right| \text{ k ohms} = 200\text{k ohms} .$$

It is apparent from Figure 40e, that r_m is at least as large as this value. It is also apparent that if R is less than this value, then a stable solution point will exist, since the load line must intersect at least one of the positive resistance regions. R_c will now be defined as the critical value of R such that $R > R_c$ is necessary for instability.

In equation form, R_c is defined as

$$R_c = \left| \frac{V_{BO} - V_h}{I_{BO} - I_h} \right| \tag{37}$$

The parameters which were determined from the device v-i characteristics are shown in Table I.

TABLE I

FOUR-LAYER DIODE PARAMETERS AS OBTAINED FROM V-I CHARACTERISTICS PRESENTED ON CURVE TRACER

Unit #	V_{BO} volts	I_{BO} ma.	V_h volts	I_h ma.	R_{off} megohms	r_m megohms	R_c Kohms	R_{on} ohms
1	28	0	0.8	9.5	13.5	0.1	2.8	1
2	24	0.04	1.0	0.16	0.57	1.0	200.0	1

It should be kept in mind that $V_{BO} < E < I_h R$ must be satisfied for instability, if R is only slightly greater than R_c, the value of E which allows this inequality to be satisfied becomes very critical, therefore, it is concluded that R should be chosen at least two times as large as R_c in any oscillator application, and preferably even larger.

Relaxation Oscillator

For the convenience of the reader, Equation (34) is reproduced here as

$$t_c = RC \ln \left| \frac{E}{E - V_{BO}} \right| .$$

The log term in Equation 34 is the ratio of the time the capacitor is

allowed to charge to the RC time constant determining the rate of charge. The linearity of the charging portion of the relaxation waveform can thus be increased by making the ratio

$$\frac{E}{(E - V_{BO})}$$

as near unity as possible. This, of course, is accomplished by making E as large as possible, while still keeping $E < I_h R$.

Unit #1

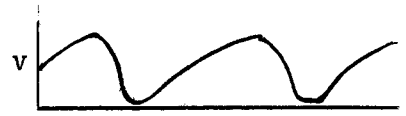
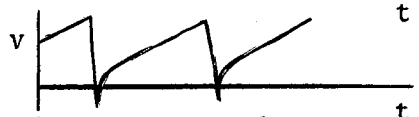
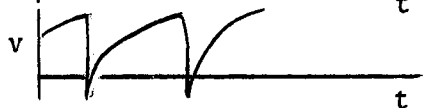
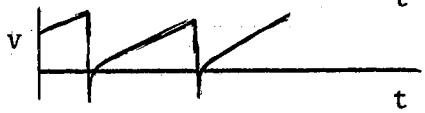
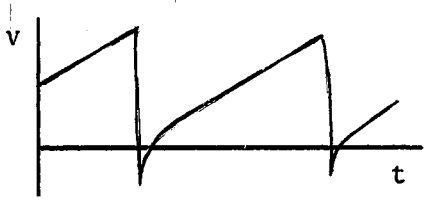
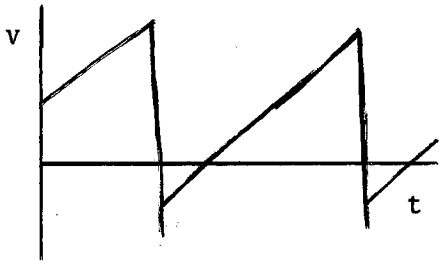
A relaxation oscillator was constructed using unit #1, and data were taken as a function of the capacitance C. The basic CNLR relaxation oscillator circuit (Figure 13) was used. Initially, a value of 15k ohms was chosen as R so as to allow some adjustment of the bias voltage. Two other values were then used to show the effect of the bias voltage. Table II shows the results obtained for various values of C and E at the three fixed values of load resistances. The charging period was calculated using Equation (34), since the conditions under which it was developed were satisfied by the parameter values of R, R_{off}, and R_{on}. For values of E sufficiently large, it is apparent that the slope of the waveform during the charging period can be nearly constant.

The overshoot at the end of the discharge period was due to an impulsive voltage being built up across the wiring inductance and self-inductance of the four-layer diode during the transistion period between the "on" and "off" conditions of the device.

A minimum value of capacitance for relaxation oscillations was found to be approximately 200 pf. For values of C less than this value, the circuit became stable in the negative resistance region, even though

TABLE II

RELAXATION OSCILLATOR EXPERIMENTAL RESULTS--UNIT #1

R	C	E	t_c	t_d	t_c	Waveform
			Measured		Calculated	
k	μf	volts	msec.	usec.	msec.	
15	0.001	36	0.027	5.4	0.023	
15	0.01	90	0.071	3.1	0.056	
15	0.01	90	0.9	1.24	0.56	
15	0.1	150	0.52	-	0.31	
27	0.1	30	9.4	0.5	11.3	
27	1.0	150	8.6	-	5.58	
100	0.01	200	0.165	-	0.15	
		300	0.68	-	0.97	
100	0.1	100	4.6	-	3.3	
		200	2.1	-	1.5	
		300	1.5	-	0.92	
		400	1.1	-	0.2	

the value of R was larger than R_c. This minimum value of capacitance is determined by the amount of energy which must be stored during the switching or transition periods. Too small a value of capacitance across the device actually makes the circuit appear as if there is no capacitance across it at all. In other words, the circuit appears as the simple series resistance and CNLR circuit biased in the negative resistance region and having $R > R_c$. This circuit is, of course, stable.

In each of the cases indicated in Table II, the oscillations were self-starting, meaning that no initial cycling of the bias voltage was required to set the circuit oscillating.

By making E large, it is apparent that a fairly linear recurrent sweep voltage can be generated. The magnitude of this voltage is approximately equal to V_{BO}, and the frequency can easily be changed by varying either the capacitance or resistance. It is preferable to change the capacitance for frequency control, since the resistance must represent the load on the circuit. Also, changes in the bias resistance have a great effect on the circuit's bias point. Changes in circuit loading could effect the circuit's bias also if the device was critically biased. Thus, maximum stability as to changes in load is obtained when the total load resistance is made much larger than R_c. A PN diode clipper could be used to clip off the transient voltage at the beginning of each sweep.

Unit #2

The same circuit was constructed using unit #2, and a load resistance of 1 megohm was used as the bias resistor. The large value of R was

required, since the region of instability was rather narrow for this unit. The best value of E was found to be approximately 175 volts. This value of voltage slightly disagrees with the criteria for instability,

$$E < I_h R$$

since $I_h R$ in this case was only 160 volts. This contradiction simply points out the difficulty in accurately determining I_h from the v-i characteristics, since the transition from negative to positive resistance at that point is not nearly as abrupt as that at the point of avalanche. Table III shows the results obtained from this circuit for different values of capacitance.

TABLE III

RELAXATION OSCILLATOR EXPERIMENTAL RESULTS--UNIT #2

Discharge time approximately 0.4 microseconds

E = 175 volts V_{BO} = 23 volts R = 1 megohm

C f	t_c measured msec.	t_c calculated msec.
0.004	0.49	0.56
0.005	0.65	0.70
0.006	0.79	0.84
0.007	0.93	0.98
0.008	1.08	1.12
0.009	1.34	1.26
0.01	1.40	1.40
0.02	3.00	2.8
0.06	9.90	8.40
0.10	17.00	14.00
0.30	54.00	42.00

The output waveform of the circuit using unit #2 was a very linear recurrent voltage sweep with less than 10 percent overshoot at the transition from "on" to "off". The discharge time was about 0.4 microseconds in each case, indicating that the transient time of the four-layer diode dominated the actual time spent in the "on" condition. Figure 41 shows the waveform of the voltage across the four-layer diode under the conditions tabulated in Table III.

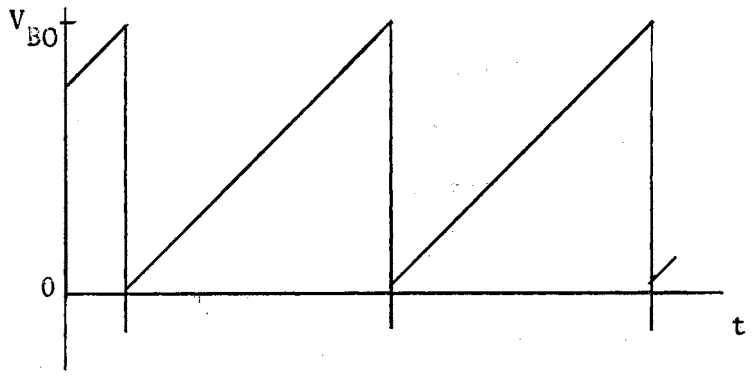


Figure 41. Relaxation Oscillator Waveform--Unit #2

An examination of the data in Table III indicates very good agreement between the measured and calculated discharge times. For values of capacitance less than 0.004 μf, relaxation oscillations similar to that shown in Figure 41 were obtained, but the waveform was not nearly as linear as that of Figure 41. The generation of high frequency sweeps appears to be limited with devices similar to unit #2, since linear sweep voltages would require very large values of E, and this in turn would require a large bias resistance due to the low value of holding current. Reference to Equation (34) indicates that the size of R places definite limitations on the generation of high frequency sweep voltages.

Sinusoidal Oscillator

The first attempt to design a sinusoidal oscillator was very discouraging. Unit #1 was used with the circuit of Figure 20, and only highly distorted, extremely low amplitude sinewave output voltages could be obtained. It was determined that the only region of the v-i characteristics of unit #1 which would support sinusoidal oscillations was that region in the negative resistance region nearest the breakover point. This is not to say that sinusoidal oscillations were not observed when the circuit was biased in other regions, for they were. The point is that relaxation oscillations predominated in all other regions and that a pure sine wave could only be obtained by adjusting the bias voltage until the device switched into the negative resistance region and then decreasing E until the load line was tangent to the v-i characteristics. The actual biasing condition is indicated in Figure 42.

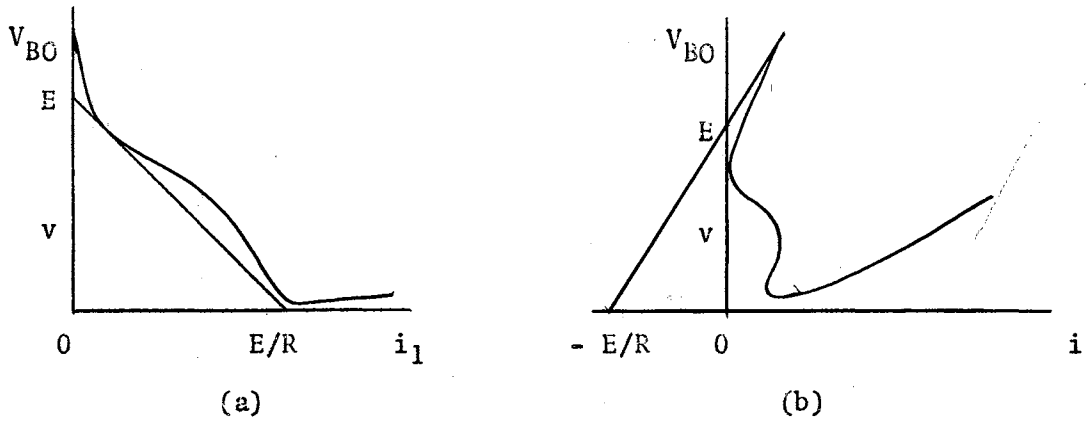


Figure 42. Biasing Condition for Sinusoidal Oscillator--Unit #1

For values of capacitance greater than 200 pf, relaxation oscillations took place, independent of the value of inductance used.

For values of capacitance less than 200 pf, as was indicated earlier in this chapter, the circuit was stable in the negative resistance region with $R > r$. In this case, by adjusting E--if R is less than r_m--then there is some region where $R = r$. The existence of sinusoidal oscillations when $R = r$ is a direct contradiction to the criteria developed in Chapter II, since it is impossible for the coordinate point (R, R) to lie in Region #1 of Figure 22. This apparent contradiction can be rationalized by citing an analogous phenomena. It is well known that a space charge or cloud of negative particles exists near the cathode of a vacuum tube. The particles which make up this space charge are continually being replaced by new particles from the cathode as they are attracted to the plate. When the space charge is considered from a macroscopic point of view, it is possible to apply mathematical statistics to the total electron stream and obtain an analysis of this phenomena. If the space charge were to be considered from a microscopic point of view, it would be impossible to predict what any individual particle's trajectory might be, or its contribution to a net space charge. Similarly, the graphical and analytical techniques developed in Chapter II may fail in certain very nonlinear regions when the region under consideration is extremely small. It appears that solution points of the v-i plot of Figure 41b where the slope of the characteristic is infinite may, therefore, be points of instability under certain terminal conditions.

The sine wave oscillator worked very well with unit #2. A value of bias resistance of 1.6 megohms was used in conjunction with a bias voltage of 110 volts. This biased the device in its negative resistance region and also allowed quite a large adjustment of the bias voltage

if required. A 106.3 pf capacitor was found to work very well with a 60 - 400 millihenry variable inductance coil which was continuously variable. No cycling of the bias voltage was required to obtain sinusoidal oscillations once the circuit was biased correctly, it being completely self-starting. Table IV indicates the data resulting from measurements taken with various values of inductance L.

TABLE IV

SINUSOIDAL OSCILLATOR EXPERIMENTAL RESULTS--UNIT #2

L mh.	T μsec.	f_m kcps	f_c kcps
100	72.0	13.9	48.7
125	74.0	13.5	43.6
150	76.0	13.16	39.8
225	80.0	12.5	32.4

No oscillations could be obtained for values of L less than 96.0 mh. When values of L greater than 225 mh. were used, the output became very distorted and began to resemble relaxation oscillations.

It is of interest to compute the value of

$$a = 2\sqrt{\frac{L}{C}}$$

for the two limiting conditions on L. With L = 96 mh., this gives

$$(\min)a = 60k \text{ ohms}$$

and with L = 225 mh. this gives

$$(\max)a = 92k \text{ ohms} .$$

Each of these values is considerably lower than any of the resistance parameters indicated in Table I for unit #2. It must be remembered though, that the slope of the v-i characteristics at the point of intersection with the load line may be much less than R_c as defined in Equation (37). For instance, it was easily determined that the minimum value of negative resistance associated with unit #1 was approximately 1k ohm, which was nearly 1/3 as large as R_c.

The value of R_c determined for unit #2 was approximately 200k ohms. It is therefore very likely that the slope of the v-i characteristics at the bias point is in the vicinity of 60k ohms. Thus, it is evident that values of L less than 96 mh. indicated that r was greater than $2\sqrt{\frac{L}{C}}$, locating the operating point (R, r) in Region #2 of Figure 22.

The frequency of the sine wave output is seen from Table IV to be approximately 1/3 of the undamped series resonant frequency determined by

$$f_c = \frac{1}{2\pi\sqrt{LC}} \quad .$$

In the case where L = 100 mh.,

$$f_c = 48.7 \text{ kcps.}$$

Recalling Equation (24), it is apparent that if the term

$$\frac{R_t^2 C}{(4L)}$$

is more than a very small fraction of unity, then the equation

$$f = \frac{1}{2\pi}\frac{1}{\sqrt{LC}}\sqrt{1 - \frac{R_t^2 C}{4L}}$$

must be used to determine the frequency. The frequency computed with L = 100 mh. and r = 60k ohms is

$$f = 16.4 \text{ kcps.}$$

Although an error does exist between this computed value and the actual observed value, it is much smaller than that obtained using the equation giving the undamped frequency. The largest source of error is, of course, the difficulty in determining the value of r at the bias point.

No other four-layer diode was available which exhibited the same type of characteristics as unit #2, or unit #1, for that matter. It appears that the new four-layer diodes which are formed by an epitaxial process, as was unit #2, will have more application as sinusoidal oscillators than the older units which have holding currents 10 to 50 times as great. A direct result of the lower holding current is the higher values of incremental negative resistance.

After many hours spent observing all types of exotic waveshapes, it is the conclusion of this author that sinusoidal oscillator applications of four-layer diodes may be limited to fixed frequency oscillators. When the bias point is located in the most linear negative resistance region and as far removed from the (V_{BO}, I_{BO}) and (V_h, I_h) points as possible, the sinusoidal oscillator circuit appears to be capable of delivering a very constant frequency output, since temperature effects do not appear to affect this region nearly as much as the points of greater non-linearity.

CHAPTER VI

SUMMARY AND CONCLUSIONS

The purpose of this thesis has been two-fold. The first portion concerned the development of a general theory of oscillations. This theory could be applied to any one-port device which exhibits an incremental negative resistance over some region of its v-i characteristics. The investigation was limited to current controlled non-linear resistances, although the theory would be equally applicable to voltage controlled non-linear resistances through a duality transformation.

This general theory, when applied to a set of v-i characteristics and a single storage element allowed the circuit designer to determine a range of values for the external biasing network and storage element which allowed a gross prediction of the output waveform and period to be made.

When at least two different types of storage elements were present in the circuit, the graphical or characteristic analysis method became unduly complicated. For this reason, a piecewise linear representation of the v-i characteristics was used.

Using the piecewise linearized model of the circuit containing two storage elements, a set of necessary conditions for oscillations of various types was determined. These conditions were plotted as four distinct regions in the (r, R) plane. R was defined as the external

circuit resistance and r as the negative internal resistance. This diagram allowed the general waveform of the output response to be predicted simply by knowing R, the slope of the v-i characteristics at the bias point, and the term $\sqrt{\frac{L}{C}}$.

The theory developed for the general current controlled non-linear resistance was then examined as to its application to the four-layer semiconductor diode characteristics. The origin of the incremental negative resistance region of the four-layer diode was determined through an analysis of junction diode and transistor properties.

To validate the oscillator theory, experimental oscillators were designed using the parameters characterizing the four-layer diode in conjunction with the general theory of oscillations.

Subject to gross non-linearities which were either linearized or neglected, the results of the experimental analysis validated in general the predicted response as to waveshape and frequency. The presence of spurious modes of oscillation were noted, indicating that the regions of particular operation in the (r, R) plane were not as distinct in the case of the extremely non-linear v-i characteristics as in the piecewise linear model.

The primary problem concerning the four-layer diode as an oscillator appears to be in obtaining a variable frequency output. As a fixed frequency oscillator, the design can be optimized and the circuit will deliver a stable frequency excitation to a load, providing the variations in loading are not so great as to change the bias point of the circuit by a large amount.

The high "off" resistance and low "on" resistance of the four-layer diode endow it with the characteristics of a slightly imperfect switch.

These extremely non-linear characteristics, therefore, lead the author to conclude that wide application exist in switching circuitry for four-layer diodes.

The utilization of negative reistance devices in monostable and bistable switching circuits was briefly discussed in Chapter II. The author believes that the graphical techniques developed in this thesis could easily be extended as an aid to the application of four-layer diodes in these switching circuits. The design of a complete set of logic circuits using four-layer diodes also appears to be very promising.

The author's advisor, Dr. Harold T. Fristoe, indicates that at least one industrial company is utilizing four-layer diodes as the tone source of an electronic organ. This appears to be an ideal application of the four-layer diode as a fixed frequency oscillator. The device's extremely small size might also make feasible its application as a tone generator for telemetry signals.

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